ED1-1-INV

Ultra-light Dark Matter Search Based on RF Quantum Upconverters

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The science reach of searches for Ultralight (sub-μeV), wavelike dark matter candidates including axions and hidden photons can be greatly enhanced by quantum sensors. At Stanford/SLAC, we are developing the Radio Frequency Quantum Upconverter (RQU), a Josephson-junction-based device capable of measuring low-frequency electromagnetic signals more sensitively than the Standard Quantum Limit. In particular, these sensors will be used to search for QCD axion dark matter in the Dark Matter Radio experiment at masses from 10neV to 1 μeV. The RQU is a quantum sensor capable of implementing multiple quantum coherent measurement techniques below 300 MHz, including two-mode squeezing, sideband cooling, and backaction evasion. I will describe the implementation of an RQU with superconducting microwave circuit elements and quantum coherent measurement protocols appropriate for ultra-light dark matter detection.

Keywords: Josephson Junctions, Dark matter search, quantum sensors

ED1-2-INV

Development of fine-pitch high-resolution hybrid TES microcalorimeter arrays toward the Lynx X-ray microcalorimeter

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We are developing hybrid transition-edge sensor (TES) microcalorimeter arrays for next generation X-ray satellite missions such as the Lynx X-ray microcalorimeter. The Lynx mission is one of four flagship mission concepts currently being studied for consideration in the National Academy of Science 2020 decadal survey. The proposed Lynx design combines a subarcsecond X-ray optic with a microcalorimeter imaging spectrometer incorporating ~100,000 pixels. The baseline design of the Lynx X-ray Microcalorimeter is a hybrid array consisting of three TES sub-arrays: main array, enhanced main array, and ultra-high-resolution array. The main array will provide 3 eV energy resolution over the 0.2–7 keV energy band with 1" pixels for 5'× 5' field of view (FOV). The enhanced main array is placed at the center of the main array and covers 1' × 1' FOV with 0.5" pixels, which will provide 1.5 eV energy resolution over the same energy band. The ultra-high-resolution array, which is placed beside the main array, covers 1' × 1' FOV with 1" pixels and will provide 0.3 eV over the 0.2–0.75 keV energy band. To match with the subarcsecond angular resolution, the pixel pitch is 50 μm for the main array and the ultra-high-resolution array and 25 μm for the enhanced main array. To reduce the number of sensors, the main array and the enhanced main array are position sensitive 5×5 multi-absorber 'hydra' microcalorimeters. Our prototype hydra array achieved 2.5±0.9 eV full-width-half-maximum (FWHM) and 3.4±1.0 eV FWHM at 1.25 keV for the 25 μm and 50 μm pitch pixels respectively, and the prototype for the ultra-high-resolution array achieved 0.3 eV FWHM at 3 eV. We will report the requirements to the detector, the concept of our detector design, and the recent achievements we have made.

ED1-3

The developments of TES array and the detector stage towards the observation from 100 eV to 15 keV for STEM

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An energy-dispersive X-ray spectroscopy (EDS) on a scanning transmission electron microscope is a useful tool for material analysis, planetary science, and other researches. We have been developing 64-pixel TES arrays as detector for the EDS system and the detector head with 3D superconducting wirings. The energy resolution is 7 eV (FWHM, at FeK¥alpha) under a few hundred cps with 17 TES pixels^{1}. In the current system, we can detect only the low energy X-ray to 0.5 keV, to improve the sensitivity below 0.5 keV to and increase statistic are required. The sensitivity for low energy depends on background level and low detection efficiency. We increase the signal-to-noise ration by improving the energy resolution of the TES with two different type TESs. On the other hands, the s statistic was limited by the number of operating pixels, in order to improve the number of operating pixels without using the 3D superconducting wirings^{2, 3}, we adopted poly-capillary X-ray optics^{4} for increasing the solid angle from the specimen and developed a detector head with simple design. In this paper we present the details of the detector head design for 64-pixel parallel readout and of the concept design of the TES array with two types of TES in the same device for the wide energy band.

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[4] A.Takano et al., 2018, doi:10.1109/TNS.2017.2786703

Keywords: TES, EDS

ED1-4

Understanding the temperature sensitivity and current sensitivity in two-dimensional transition-edge sensor film

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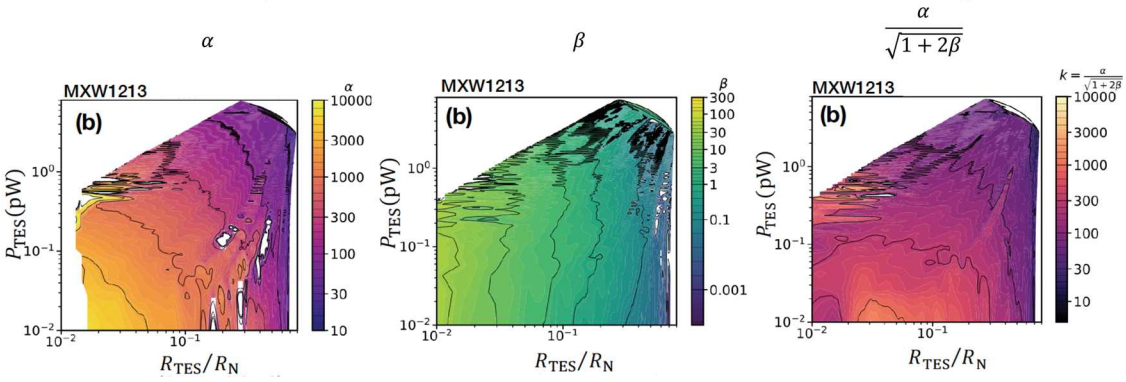
Transition-edge sensor fabricated by normal-superconducting bilayer is widely applied to X-ray spectrometers and infrared to sub-mm image sensors with the aim of potentially unprecedented high energy resolution and sensitivities. As a key component of the X-ray microcalorimeter, the transition-edge sensor has two main parameters that affect the energy resolution, temperature sensitivity and current sensitivity. Tremendous efforts have been made to fabricate transition-edge sensor with high temperature sensitivity and low current sensitivity in order to enhance the energy resolution of the detectors. However, since the resistance of the transition-edge sensor is a complex function of temperature, current and magnetic field, we were lack of systematic knowledge of the resistive surface in its superconducting transition, which has prevented us achieving an optimized operational point of the detector. We thus conducted an experiment to map the resistance, temperature sensitivity and current sensitivity of the transition-edge sensor in its complete superconducting transition, in order to understand if/how the temperature sensitivity and current sensitivity are correlated with each other and where to identify the global optimized bias point to achieve the best energy resolution. As a result, the experimental evidence suggests that the current sensitivity depends only on the resistance of the transition-edge sensor, which supports the prediction of the two-fluid model. With the concept of the phase-slip center as a resistive mechanism, we demonstrate that the figure of merit of the energy resolution as well as the current sensitivity are both correlated with the quasiparticle diffusion length.



Keywords: Transition-Edge Sensor, Energy Resolution, Current Sensitivity, Two-fluid model

ED2-1-INV

Energy-Resolved Neutron Imaging using a Delay Line Current-Biased Kinetic-Inductance Detector

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Superconducting detectors are one of the most successful superconducting applications [1]. It has an advantage in high sensitivity and fast response, and has been applied to the detection of cosmic rays and single photons [2]. We have been developing a unique superconducting neutron detector, called current-biased kinetic-inductance-detector (CBKID) [3,4]. Our detector comprises *X* and *Y* superconducting Nb meander lines with Nb ground plane and a ^{10}B neutron conversion layer, which converts a neutron into two charged particles. High-energy charged particles (α particle or ^{7}Li particle) are able to create hot spots simultaneously in the *X* and *Y* meander lines, and thus, the local Cooper pair density in meander lines are reduced temporary. When a DC-bias currents are fed into the meander lines, pairs of voltage pulses are generated at hot spots and propagate toward both ends of the meander lines as electromagnetic waves. The position of the original hot spot is determined by a difference in arrival times of the two pulses at the two ends with a spatial resolution of the order of the meander repetition length for *X* and *Y* meander lines, independently. This is so-called the delay-line method, and allows us to reconstruct the two-dimensional neutron transmission image of test patterns with four signal readout lines.

CBKIDs can handle multi-hit events, and the typical signal width was a fen tens ns. Hence, we estimate the detection-rate tolerance to be as high as a few tens MHz. Therefore, energy resolved-neutron imaging is available with the combination of the time-of-flight technique in pulsed neutron sources.

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Keywords: Superconducting detector, Kinetic inductance, Neutron imaging

ED2-2-INV

Development of SEM-EDS analyzer utilizing 100-pixel superconducting-tunnel-junction array X-ray detector toward nanometer-scale elemental mapping

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An energy-dispersive X-ray spectroscopy (EDS) analyser combined with a scanning electron microscope (SEM) is suitable to obtain spatial and quantitative information on the elemental composition of a sample non-destructively. In particular, low-acceleration-voltage SEMs (LVSEMs) theoretically allow evaluating those informations of a sample with a nanometer lateral resolution [1]. However, it isn't suitable to use conventional EDS analysers such as silicon drift detectors (SDDs) for obtaining X-ray spectra from samples in LVSEMs, because emitted X-ray from samples in LVSEMs are only soft X-ray and the energy-resolving power of conventional energy-dispersive X-ray detectors is insufficient to clearly resolve such soft X-rays. On the other hand, wavelength-dispersive X-ray spectrometer (WDS) can be resolved the soft X-rays because its energy resolution is less than 10 eV. However throughput of the WDSs is very low.
In contrast, energy-dispersive X-ray detectors based on superconducting-tunnel-junctions (STJs) have simultaneously exhibited excellent energy resolution of <10 eV, relatively large detection area of >1 mm^2, and high counting rate capability of >200 kcps for soft X-rays less than 1 keV [2]. We have developed the SEM utilizing STJ array as an EDS analyzer [3], which is abbreviate as SC-SEM hereafter, in order to realize nanometer-scale elemental mapping.
Fig. shows a picture of the SC-SEM. The SC-SEM consisted of a field emission SEM and a 100-pixel STJ array X-ray detector. X-rays emitted from the sample by the electron beam were detected by the STJ array via the polycapillary X-ray lens and two X-ray windows. The enegry resolution for N-Kα of the STJ (12 eV) was about 5 times higher than that of the SDD (60 eV). The throughput for N-Kα of the STJ was about 50 times smaller than that of the SDD. In the future, by improving the X-ray optics, the throughput is expected to be increased about 10 times. The SC-SEM can perform nanometer-scale elemental mapping because the SC-SEM realizes both the high throughputs of SDDs and the excellent energy resolution of WDSs.

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Fig. Picture of the SC-SEM

Keywords: SEM-EDS, Superconducting tunnel junction, X-ray, nanometer-scale

ED2-3-INV

HTS-SQUID module with high tolerance to magnetic field and its application

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We developed an HTS-SQUID module applicable to various systems [1]. The SQUID module was designed to connect an external pickup coil suitable for each application. The hermetically encapsulated SQUID module includes an HTS planar gradiometer and an HTS multi-turn input coil, which are fabricated on separate substrates and stacked together. Since the SQUID module can be magnetically shielded to avoid exposure to external magnetic field, a stable feedback operation is possible under severe conditions such as strong excitation field and/or motion in the Earth's field. The SQUID modules have been used in a bioassay system based on ac magnetic susceptibility measurement [2], moisture content measurements of rice kernels and soil utilizing diamagnetic characteristics of water [3], magnetic particle imaging [4, 5] and so on. Recently, we have developed a three-channel SQUID eddy current testing (ECT) system on a hand cart for detection of a fatigue crack in a steel deck plate under an asphalt pavement used in an expressway bridge [6]. We could demonstrate a stable long-time operation of the ECT system on an expressway bridge in an urban area during the daytime and acquisition of correct data corresponding to some structural features of the expressway bridge.

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Keywords: SQUID, Nondestructive evaluation, Biological diagnosis , Eddy current testing

ED2-4

Development of scanning SQUID microscope system and its applications on geological samples: A case study on marine ferromanganese crust

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We present developments and applications of a high-resolution scanning superconducting quantum interference device (SQUID) microscope for imaging the magnetic field of geological samples at room temperature. The scanning SQUID microscope (SSM) uses a hollow-structured cryostat. A directly coupled low-temperature SQUID with a 200 μm × 200 μm pickup loop, which is mounted on a sapphire conical rod, is separated from room temperature and atmospheric pressure by a thin sapphire window. Precise and repeatable adjustment of the vacuum gap between the SQUID and the sapphire window is performed by rotating a micrometer spindle connected to the sapphire rod through the hollow portion of the cryostat. When the SQUID was operated in superconductive shield with the low-drift FLL, we obtained a field noise of 1.1 pT/√Hz at 1 Hz. While the typical environmental noise of the system operated within the two layered PC permalloy is about 50 pT. Environmental noise is reduced by subtracting a signal from a reference SQUID that is placed inside a cryostat. A geological thin section is placed on top of a non-magnetic sample holder with an XYZ stage that enables scanning of an area of 100 mm × 100 mm. The minimum achievable sensor-to-sample distance is measured as ~200 μm. The new instrument is a powerful tool that could be used in various geological applications.

A successful application of the SSM to a marine ferromanganese crust will be shown. Marine ferromanganese crusts are marine ore deposits rich in rare earth elements. They grow slowly and record long-term deep-sea environmental changes. We conducted magnetic field mapping with the SSM on a crust sample from northwestern Pacific and found beautiful stripes in the magnetic field images. It is known that the Earth's magnetic field experienced polarity changes in the past. Because the major polarity changes were studied well and the ages were determined with the other methods, we could make use of the boundaries of magnetic field changes to estimate an age of a deposition (a technique known as "magnetostratigraphy"). By correlating the obtained profiles with a standard geomagnetic polarity timescale, we obtained an average growth rate of several mm/Ma, which is consistent with that obtained by radiometric dating.

Keywords: Scanning SQUID microscope, magnetic field imaging, geological applications, marine ferromangense crust

ED3-1-INV

Digital Applications with High-T_c Superconductors

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One of the early predictions for high-T_c superconductors was their application in digital systems. Not only would the power consumption for cooling be down by a factor of 100, but also the achievable clock rates would be much higher. At that time, the prospects for high-current applications were quite pessimistic. Nowadays, the situation is reversed: the prospects for high-current applications are excellent, especially for magnets, and the prospects for high-T_c digital applications are dim. There reasons are partially technology related, but also related to the needs of the society - complex material issues require big investments and such investments are easier to defend for a room temperature technology than for a cryogenic one: until the need arises that can only be solved by a cryogenic technology. But there is no need to wait, quite a number of applications have successfully been demonstrated in the past. And there are still quite a number of applications around that can be solved with the current technology or with technologies which will mature soon: grain-boundary junctions either on bi-crystals or on step-edges allow the preparation of circuits with a small number of junctions and direct writing of Josephson junctions may yield a tool to create an even larger number of Josephson junctions for digital applications. Since currently only thin film covered substrates with one or two layers of high-T_c superconductors are commercially available, the selection of the right family of Josephson digital circuits is in this context essential.

Keywords: Superconductivity, Digital Devices, High-T_c, Josephson Junctions

ED3-2-INV

Topological superconductivity – new materials for novel devices

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The interplay of induced superconductivity and Dirac physics at the interface of an s-wave superconductor (S) and a 3D topological insulator (TI) turns the surface of the TI into a 2D topological superconductor. Different to conventional superconductors, topological superconductors host exotic subgap states – so-called Majorana modes – at zero energy. In order to employ Majorana modes in future fault-tolerant topological quantum computers, high quality S–TI hybrid devices are required. For achieving pristine interface quality we exploit stencil lithography for full *in situ* fabrication of S–TI hybrid devices via molecular-beam epitaxy. As-prepared Josephson junctions show highly transparent S-TI interfaces and Shapiro response measurements indicate the presence of gapless Andreev bound states, so-called Majorana bound states. To move from single junctions towards complex circuitry for future topological quantum computation architectures, we monolithically integrate two aligned hard masks to the substrate prior to molecular-beam epitaxy. The so-called Jülich process allows to fabricate complex networks of topological insulators and superconductors *in situ* with nm precision.

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Keywords: Topological superconductivity, Majorana, Topological insulator, Molecular-beam epitaxy

ED3-3-INV

Filling and Bridging the THz Gap Using High-T_c Superconducting $Bi_2Sr_2CaCu_2O_{8+\square}$ Intrinsic Josephson Junction Emitters

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Generation of terahertz (1 THz=10^{12} c/s) electromagnetic waves with a frequency range of 0.3 – 10 THz in-between microwaves and infrared light in the electromagnetic spectrum has been a long-standing issue in the history of optics and optical science and engineering. Recent rapid progress in information technology over the wide frequency spectrum of the electromagnetic waves has urged researchers for the development of TBit technologies. In addition, the demand for the THz waves has also been grown to overcome first the technological barrier to generate THz waves. During last two decades enormous effort has been made. As a result, semiconductor devices such as RTD or QCL devices have been developed successfully. At present, the out-put power of ~1 μW at 1.42 THz by RTD[1] and 0.36 mW at 1.4 THz by cold QCL at 10 K[2] have been reported. Although the THz gap gets narrower and narrower and the valley becomes shallower and shallower, a great difficulty still lies there and hinders many interesting applications in this frequency range.

A new challenge has been started in 2007 after the discovery of continuous and coherent THz emission was discovered in an intrinsic Josephson mesa device fabricated on the single crystal substrate of high temperature superconductor $Bi_2Sr_2CaCu_2O_{8+\delta}$, which is well-known as highly 2D anisotropic layered superconductor. Using multi-stacked Josephson layer property, we could manage to develop THz emission up to 2.4 THz[3].

Just recently, we have successfully made a remarkable improvement on high frequency properties by making a new type of devices. We think that this type of devices may be ultimate conceptually and can be applied in the arrays easily. This progress will be reported in my talk together with the recent work on the applications using algae paramylon and the related carbohydrates such as cellulose, curdlan, etc.

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ED3-4-INV

Proposal and Fabrication of Hot Electron Bolometer Mixer using a Magnetic Thin Film

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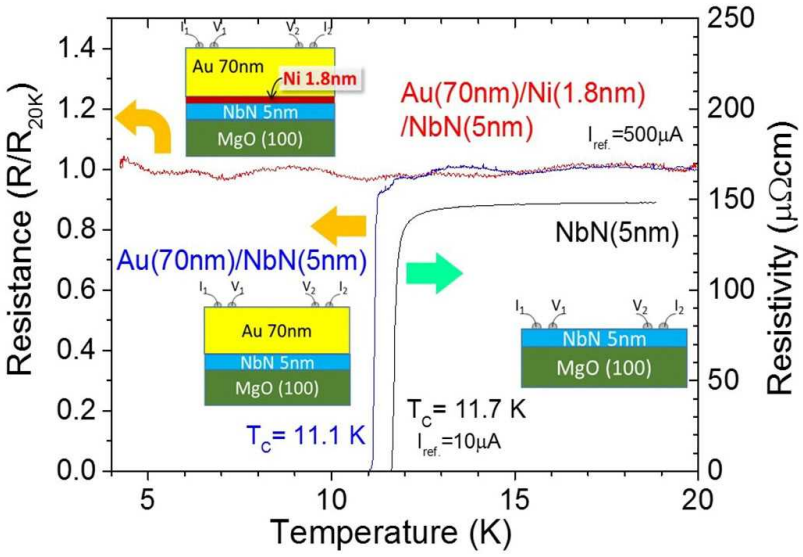
Hot-electron bolometer mixers (HEBMs) are expected to replace SIS mixers as extremely low-noise mixer in applications beyond 1.5 THz. However, the IF bandwidth of an HEBM remains limited to typically 3–5 GHz and it is not sufficient when compared to that of an SIS mixer. Therefore, we proposed a new HEBM structure (Ni-HEBM) using a nickel (Ni) magnetic thin film [1]. Ni-HEBM aims to expand IF bandwidth and improve sensitivity by miniaturizing HEBM which was realized by the controlling the superconducting region with Ni thin film.

HEBM structure comprises with a thin superconducting strip placed between two metal electrodes, and it uses a sudden impedance change in the superconducting transition of the strip. To ensure a good electrical contact, the strip and both electrodes are usually connected via an overlap region on the strip. However, usually superconductivity remained in the region and it has been prevented the miniaturization of conventional HEBM. We found that it is possible to suppress the superconductivity of the niobium nitride (NbN) thin film by the addition of a Ni thin film. Figure shows the temperature dependence of the resistance of the Au (70 nm)/ Ni (1.8 nm)/ NbN (5 nm) trilayer for forming the overlap region of the Ni-HEBM electrodes. For comparison, another bilayer of Au (70 nm)/NbN (5 nm) was prepared (without Ni), which is the structure used for electrodes in a conventional HEBM. The Au/Ni/NbN trilayer film did not show superconductivity until 4.2 K. However, the Au/NbN bilayer film showed superconductivity at 11.1 K.

We fabricated Ni-HEBM with a NbN strip of 0.1 μm-length, and the IF bandwidth was evaluated at 1.9 THz. We confirmed that the IF bandwidth expands, and it was evaluated about 6.9 GHz at 4 K. The uncorrected receiver noise temperature of same Ni-HEBM was also evaluated at 4 K, and it was about 1220 K(DSB) at 2 THz.

Figure. Suppression of the NbN superconductivity under the HEBM metal electrode due to the insertion of the Ni thin film.



Keywords: HEBM, IF bandwidth, Ni, THz

ED4-1-INV

EDA for Superconducting Circuits

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Superconducting integrated circuits have long been completely handcrafted or at best designed with a loose collection of tools that require manual manipulation of data and design transfer between tools. Electronic Design Automation (EDA) software development requires significant investment of resources to track the evolution of integrated circuit fabrication processes, which has only been possible commercially for highly successful semiconductor integrated circuit processes. The IARPA SuperTools project which started in 2017 is the largest known investment to date made in superconducting EDA tool development. SuperTools is divided into two main categories: high-level tools for the synthesis of digital logic circuits, clock networks and placed-and-routed layouts for systems such as processors with millions of logic gates; and physical-level tools for the design, simulation, optimization, verification, layout and parameter extraction of devices and digital logic cells with the inclusion of fabrication process simulation. In this paper the physical-level tools are presented by way of a design example, from device characterization through logic circuit conception and design to layout verification and cell library sign-off.

ED4-2-INV

Superconducting SFQ Circuits Research Progress in China

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Although it has been about 30 years since the birth of superconducting circuits, research activities on them have remained quietly in China, if not none, until recently. The first wafer-level single flux quantum (SFQ) process in China appeared about 3 years ago at SIMIT. Since then, we have gone through several upgrades and changes. Corresponding design and measurement infrastructure have been developed on site simultaneously to enable close-loop feedback research cycles. In particular, we have established process control monitor (PCM) analysis for the latest SIMIT Nb03 SFQ process, and carried out systematically measurement and verification of cell libraries optimized for this process and move towards benchmark circuits demonstration, such as shift register, frequency divider and so on. Besides, EDA tools for optimization and buildup of SFQ cell libraries: model, behavior and timing libraries, as well as automatic placement and routing for large scale SFQ circuits design have been developed. In this report, we will present these latest progresses.

Keywords: SFQ, SFQ process, EDA Tools

ED4-3-INV

Performance Improvement of Superconducting Circuit by Introducing π-Shifted Josephson Junctions

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Hybridization of Josephson junctions (JJs) and π-shifted Josephson junction (π-JJs), which induces the static superconducting phase shift of π across the junction, is one of effective methods to improve the performance of superconducting integrated circuits. We can reduce circuit area of the superconducting circuits by replacing the large inductances with the π-JJs. Moreover, we can drastically simplify the circuit structure of superconducting flip-flop with complementally outputs by using a symmetric storage loop composed of both the JJ and the π-JJ. We will discuss the improvement of performances of superconducting circuits by introducing π-JJs into the conventional superconducting circuits quantitatively in terms of the circuit area, the operating margin, and the operating frequency on the basis of the analog circuit simulations by the PJSIM we developed. We will show a possible application to superconducting single-flux-quantum containing π-JJs to dual-rail circuit that can remove static power consumption.

Keywords: SFQ circuit, π-Josephson junction, circuit simulator

ED4-4

Enhanced Voltage Swing of RSFQ Output Amplifiers Equipped with Double-Stack SQUIDs

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We have enhanced voltage swing of an RSFQ distributed amplifier by replacing a SQUID, which works as a voltage generator, with a double-stack SQUID. A double-stack SQUID is a 4-junction SQUID with two superconducting loop. In other words, it is composed of two stacked SQUIDs sharing a sensing inductor. Because of its stack structure, a double-stack SQUID is expected to generate two-fold output voltage. We have designed 4-, 12-, and 24-stage RSFQ distributed amplifiers equipped with 4, 12, and 24 double-stack SQUIDs, respectively. The fundamental cell, of which the dimensions are 80 by 80 μm², is compatible with an RSFQ digital cell library referred to as "CONNECT." Test chips were fabricated using a 25-μA/μm² Nb integration process of the National Institute of Advanced Industrial Science and Technology, which was referred to as the AIST STP2. In measurements, a test chip was cooled in a liquid helium bath. The experimental output voltage swings of 4-, 12- and 24-stage RSFQ distributed amplifiers were up to 2.93, 8.34, and 14.50 mV, respectively.

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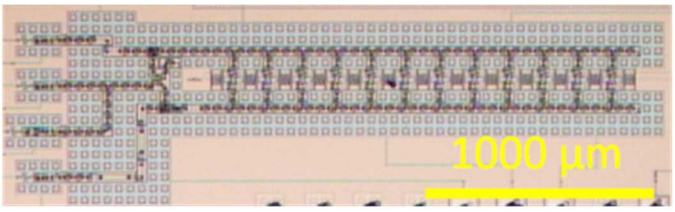
This work was partially supported by JSPS KAKENHI Grant Number 17K04979, and also by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.



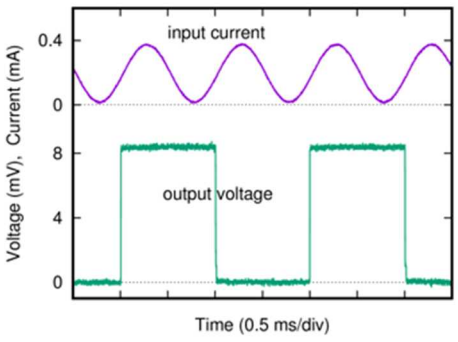


Fig. Photomicrograph and operation waveforms of a 12-stage RSFQ output amplifier equipped with double-stack SQUIDs.

Keywords: distributed amplifier, Nb/AlOx/Nb, RSFQ digital circuits, IO interface

ED4-5

Logic Simulation Tool for RSFQ Circuits Accepting Arrivals of Multiple Pulses in a Clock Period

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RSFQ circuits and their energy-efficient derivatives are expected to realize high performance and energy-efficient computers. RSFQ circuits use pulse logic. Namely, voltage pulses are used for calculating logic functions.

Logic simulation of RSFQ logic circuits is carried out after designing layouts because the order of pulse arrivals at each gate affects its logic function and the order of pulse arrivals is determined in layout design. Though design exploration in logic design with logic simulation is necessary to obtain a reasonable design, it is difficult to evaluate various designs because designing a layout is a hard task. Methods to simulate a logic design before layout are crucial. A description method of RSFQ logic circuits was proposed. In the method, the order of pulse arrivals is annotated for each gate to represent the circuit behavior explicitly. A logic simulation tool for circuit descriptions based on the method has been also shown. The method and the tool are designed for simple designs. Designs with complex orders of pulse arrivals, i.e., appearances of multiple pulses at an input terminal during a clock period, cannot be represented with the method because it assumes at most one pulse arrives at an input terminal during a clock period.

Logic functions can be implemented with fewer logic gates by utilizing complex ordering of pulse arrivals. For example, a logic function “ab’+c” can be realized simply with a confluence buffer (CB) and a resettable D flip-flop (RDFF) having data, reset, and clock input terminals. Pulses of “a” and “c” are merged with a CB and are fed to the data terminal of an RDFF and a pulse of “b” is designed to be fed to its reset terminal between the pulse arrivals of “a” and “c.” This design cannot be described with the method.

The method to be proposed is an extension of the description method to treat designs with the complex ordering of pulse arrivals. The proposed method attaches a list for each input terminal of a gate to represent the order of pulse arrivals for multiple pulses for the terminal. The list for a pin contains integers to represent the order of pulses fed for the pin in a gate during a clock cycle.

A logic simulation tool was implemented. It is written in Python. With the tool, circuits with complex orders of pulse arrivals like the above example were simulated.

Keywords: Rapid Single Flux Quantum Circuits, Logic Simulation, Design Automation

ED4-6

Design and High-speed Test of an SFQ-based Single-chip FFT Processor

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Fast Fourier transform (FFT) processor is custom hardware for computing discrete Fourier transform (DFT) at high speed, where DFT can convert a signal from a time domain to a frequency domain, and is widely used in digital signal processing. High-performance FFT processors based on single flux quantum (SFQ) circuits are attractive in many fields because of their high-speed operation with low power consumption [1]. In our previous study, we have designed and implemented a 4-bit 8-point SFQ FFT processor using the AIST 10 kA/cm^2 Nb advanced processor (ADP 2.2) [2] and confirmed the correct operation of the first stage at low-speed test [3]. In this study, we designed a 7-bit 8-point SFQ-based single-chip FFT processor and fabricated it using the ADP 2.2 process. The correct operation of the FFT processor was confirmed at the on-chip high-speed test [4]. We input 8-point discrete time-domain signals such as a sine wave and a cosine wave and demonstrated the spectrum analysis ability of the FFT processor. The FFT processor can perform 2.55×10^{11} times of FFT calculations per Joule at the maximum frequency of 47.8GHz, where it takes 7.4 ns for one time of FFT calculation. We also evaluated the energy efficiency of a 32-bit 64-point SFQ FFT processor and compared it with that of a CMOS FFT processor under a 45 nm technology. We confirmed it is two orders of magnitude better than that of the CMOS FFT processor with serial architecture.

Keywords: single flux quantum circuits, FFT, processor, superconducting

ED5-1-INV

Deterministic generation of entanglement with up to 20 superconducting qubits

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Here I will review our recent activities on designing and fabricating superconducting circuits which integrate up to 20 qubits for scalable quantum information processing. In particular, I will introduce a superconducting quantum processor featuring 20 individually-accessible Xmon qubits that are controllably coupled to a bus resonator, based on which we deterministically produce an 18-qubit Greenberger-Horne-Zeilinger state and multi-component atomic Schrödinger cat states of up to 20 qubits. We verify genuine entanglement with simultaneous measurements of all qubits involved. With the excellent control developed in our experiment, our multiqubit superconducting circuits may provide a promising platform for simulating the intriguing physics of quantum many-body systems.

Keywords: Superconducting qubit, Entanglement, Quantum information processing

ED5-2-INV

Generation and detection of itinerant microwave photons using a superconducting qubit

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A quantum network based on itinerant microwave photons is an indispensable tool to make it easier to implement a large-scale quantum computer with superconducting qubits [1]. In this talk, we show the experimental results on the generation and detection of itinerant microwave photons by using a circuit quantum electrodynamical system, where a microwave cavity plays a crucial role in facilitating the interaction between itinerant microwave photons and a superconducting qubit [2].

First, by utilizing a microwave-assisted interaction between a superconducting qubit and a cavity mode, we generated a single-photon state in a propagating mode [3]. Moreover, we extended the generation scheme to a time-bin photonic qubit, a superposition of a single photon in two orthogonal temporal modes, which can be robust for the propagation loss. Second, we implemented a deterministic entangling gate between a superconducting qubit and an itinerant microwave photon reflected by a cavity containing the qubit. Using the entanglement and high-fidelity qubit readout, we demonstrated a quantum non-demolition detection of a single photon, a photon detection without absorbing the photon energy [4].

These results on itinerant microwave photons can be a building block for the quantum network connecting distant qubit modules. Furthermore, the generation and detection of a quantum state of itinerant microwave field have promising applications for quantum sensing and metrology in the microwave regime [5].

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ED5-3-INV

Scalable packaging and wiring for superconducting quantum computers

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Superconducting qubit devices are one of the promising candidates for realizing large-scale quantum computer. The next challenge toward building quantum computer would be implementation of quantum error correction. To implement realistic quantum error correction codes, such as surface codes, we need to prepare two-dimensional array of superconducting qubits in a scalable way. It naturally requires three-dimensional wiring to superconducting qubits, which suppose to have at least one microwave control line for every qubit. A lot of efforts have been made recently to establish three-dimensional wiring techniques which ensure scalablility of superconducting qubit devices. The techniques include flip-chip bonding [1], through-silicon vias [2], contact probes [3], and direct coaxial cable wiring [4].

In this talk, we present a way to realize scalable packaging and wiring for superconducting qubits by using direct vertical interconnect between superconducting circuits and coaxial cables. The design of our package is shown in Fig. 1. In our package, coaxial cables for qubit control and readout are directly wired from the bottom of the superconducting qubit chip. The electrical contact between superconducting circuits and coaxial cables are provided by contact probes. The electromagnetic fields from the cables are guided by through-silicon vias and transmitted to the superconducting circuits on top of the chip. This wiring scheme is fully vertical and two-dimensionally scalable. We report the results of characterization of the package and measurements of the multi-qubit chip in this package.

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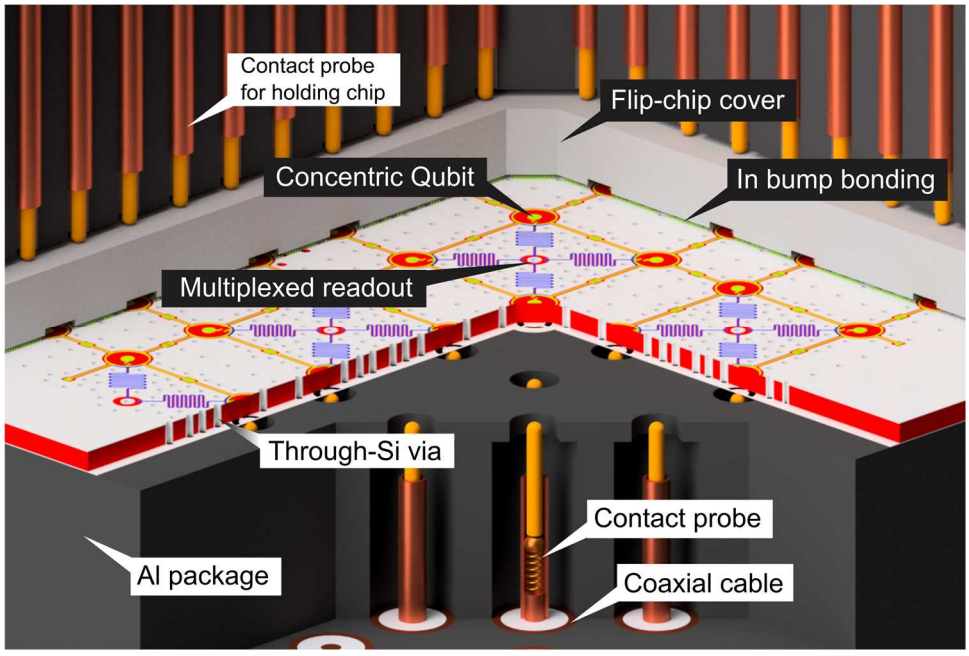

Keywords: Quantum computing, Scalable qubit packaging, Vertical interconnects

ED5-4

The Superconducting Flux Qubit for Prime Factorization Utilizing Low Jc Process

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Specific device for prime factorization utilizing a quantum annealing has been investigated[1].In this architecture, a multiplier plays an important role because its inverse operation corresponds to the prime factorization. To demonstrate this concept, we fabricated a qubit cell, which was an element of the multiplier, utilizing multi-layered Nb/AlOx/Nb Josephson junction technology with current density of 1 μA/μm^2. The cell was consisted of a superconducting flux qubit, a quantum flux parametron (QFP) and superconducting quantum interference devices (dc-SQUID) as shown in Fig. 1(a). I_c and β_L of the qubit were 6 μA and 2.8, respectively. In order to modify an energy potential, the qubit was coupled with current paths of I_{trans} and I_{Qubit}. Prior to experiments at 4.2K, bias conditions of the QFP and readout-SQUIDs were analyzed by SPICE.

At first, bias to the readout SQUID was adjusted so as to respond zero or constant value depending on a direction of a magnetic flux. Then, a current I_{QFP}, corresponding to the flux $\Phi_0/2$, was applied to the QFP. Figure 1(b) shows output signals in the readout SQUID after applying the current I_{qubit}. Here, the signals were obtained every increment of 2 μA and averaged in 20 times. Repetitions of high and zero voltage were obtained. The feature was consistent with the SPICE analysis. This indicated successful detection of the flux in the qubit where direction of a circulating current was modified by current I_{qubit}. We consider this qubit cell has possibility of constructing the multiplier for prime factorization.

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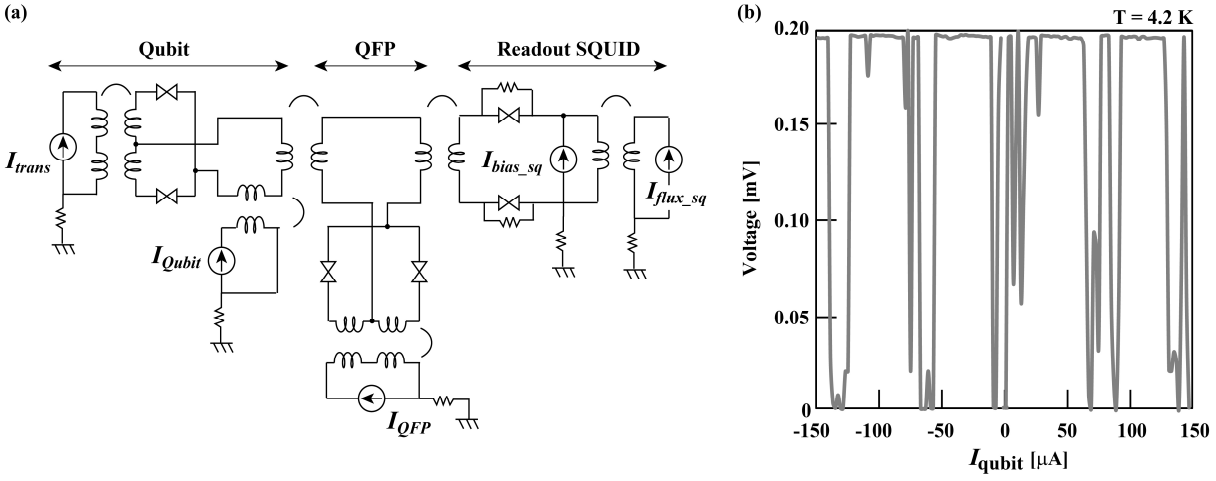
Acknowledgements

This paper is partly based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO), Japan. The devices were fabricated in the clean room for analog-digital superconductivity (CRAVITY) in National Institute of Advanced Industrial Science and Technology (AIST).



Keywords: superconducting flux qubit, Josephson junction, SQUID, quantum annealing

ED6-1-INV

High Sensitivity Nuclear Magnetic Resonance Spectroscopy Using HTS Resonators

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Nuclear magnetic resonance (NMR) is a powerful and widespread method for the detection of molecules and the determination of molecular structure. However, it has a relatively poor sensitivity compared to other techniques such as mass spectrometry. The very narrowband NMR signals are typically observed by Faraday induction in a resonant detector which is noise matched to a low noise preamplifier. In today's laboratory magnets, the NMR resonance bands of interest may be anywhere between ~40 MHz to above 1 GHz. For the most commonly observed isotopes, ^{1}H, ^{13}C, and ^{15}N resonance frequencies are very close to 10:2.5:1 ratio. We have improved the sensitivity of several spectrometers by using high-Q HTS resonators [1]. Some of the opportunities and challenges involved in using these resonators as NMR detectors will be presented.

An example of a useful resonant structure is the counterwound spiral shown in fig. A. Spirals of opposite helicity are patterned on a double-side coated wafer to produce a low frequency resonator for nuclides such as ^{13}C or ^{15}N. The relative orientation of the spirals confines most of the electric field within the dielectric substrate, reducing the electric coupling to the sample. This is important because NMR samples can be electrically lossy and are typically near room temperature. However, the high Q factor of the resonator limits both the reception and excitation bandwidth, requiring the use of techniques such as overcoupling and Q switching [2].

The HTS resonators are mounted to a cold head on either side of a liquid sample as shown in fig. B. In probes such as described in [1] there may be two or more sets of nested resonator pairs tuned to different frequencies, and interactions between the resonators must be taken into account. Problems also occur if the higher modes of ^{13}C transmission line resonators such as shown in fig. A are close to the ^{1}H resonance. Fortunately, modifications to the design of the transmission line resonator can be used to adjust its dispersion and move the modes away from other frequencies of interest [3].

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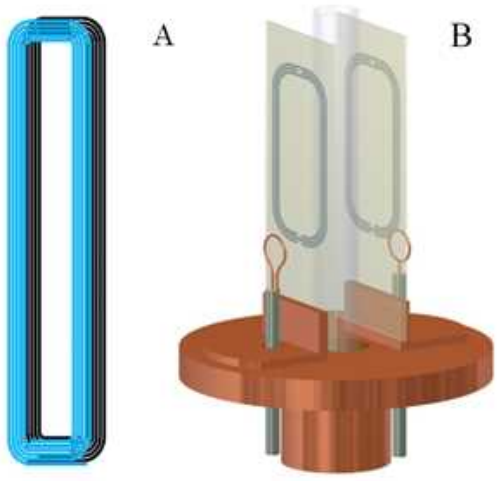

Fig. A. Counterwound spiral resonator; B. HTS resonators on both sides of the sample.

Keywords: Nuclear magnetic resonance, High-temperature superconductors, Superconducting devices

ED6-2-INV

Compact and High Performance Microwave Superconducting Bandpass Filters Using Microstrip Multimode Resonators

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As the key passive component in the radio-frequency (RF) front-end, bandpass filter (BPF) with compact size and high performance are in great demand for enhancing system functionality. Meanwhile, high-temperature superconducting (HTS) materials are becoming more and more attractive in the context of designing microwave filters because of their lower losses and excellent performance.
In past few years, several types of high performance HTS BPFs have been designed for demonstration. For circuit size miniaturization, various microstrip multimode resonators have been proposed, such as the multi-stub-loaded resonators and square ring loaded resonator. At first, a series of the second-order multiband HTS filters have been presented based on the multi-stub-loaded resonators [1], [2]. The measured insertion losses are all extremely small, but the selectivity and stopband performance need to be improved because of the low-order design. Therefore, a newly dual-mode hairpin ring resonator is proposed and applied to constitute an eighth-order dual-band HTS BPF [3]. The configuration of the designed filter and the obtained frequency responses are respective shown in Fig. (a) and (b). As predicted, the band edge selectivity and the attenuation in stopband are highly enhanced.
In addition, the differential circuits have been received much attention recently due to their ability of lower electromagnetic noise and crosstalk. So, based on the HTS technology, a fourth-order differential dual-band HTS BPF has been designed using the proposed square ring loaded resonator [4]. The layout of the differential filter is depicted in Fig. (c) and the simulated results as well as the measured results are shown in Fig. (d). It is seen from Fig. (d) that a favorable common-mode (interference signal) suppression over a wide frequency range is obtained.
With the advantages of ultra-low in-band insertion losses and high selectivity, these proposed filters are attractive for potential applications in multiband communication systems requiring high-sensitivity and high anti-interference properties.

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ED6-3-INV

Development of High-Temperature Superconducting Pick-up Coils for Field-Swept Nuclear Magnetic Resonance

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Nuclear magnetic resonance (NMR) can obtain rich information concerning molecular properties including local molecular structures and dynamics. High-temperature superconducting (HTS) pick-up coils for NMR are useful for detecting very low level RF signals. Some research groups have studied and used these coils from 40 to 700 MHz [1-3]; however, systematic research on the quality factor of the coils and detection frequency has not been done.

In this paper, we investigated the frequency dependency of unloaded quality factors, Q_u, for Cu and HTS pick-up coils by using electromagnetic simulation from 40 to 700 MHz. From the results with one-turn coils, the Q_u values assuming Cu coils were proportional to 1⁄2 the frequency power, and those assuming HTS coils were inversely proportional to the frequency. These results could be explained by the definition of the quality factor and microwave losses in normal metal and HTS material. In comparison, the Q_u values of square-spiral Cu and HTS coils significantly increased as frequency decreased below 100 MHz. Additionally, the total length of these coils was less than that of the one-turn coils at the same resonant frequency. These results indicate that square-spiral coils with a low-resonant frequency have higher Q_u values and are advantageous as miniaturized coils.

Next, we designed and fabricated HTS pick-up coils at around 40 MHz for a field-swept solid-state NMR. A square-spiral shape with a 100-μm line and 100-μm spacing was used for the coils and put on a 25 × 25 mm^2 dielectric substrate. We analyzed the S_{11} reflection, quality factors, and electromagnetic field and found that the simulated resonant frequency was around 40 MHz and the Q_u values of the coils exceeded 3×10^4. We then fabricated coils with 250-nm-thick YBCO thin films deposited on CeO_2-buffered r-sapphire substrates. The coils were patterned with laser lithography and dry-etching techniques. The S_{11} reflections of the coils were measured with a loop antenna, vector network analyzer, and cryostat. A resonant frequency of 38.525 MHz and Q_u of more than 1.6×10^4 were obtained at 9 K in a magnetic field of 3.6 T. Details will be presented at the conference.

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Keywords: NMR, Pick-up coil, YBCO thin film

ED6-4

Required Characteristics of YBCO Thin Films to Fabricate High-Q NMR Pickup Coils

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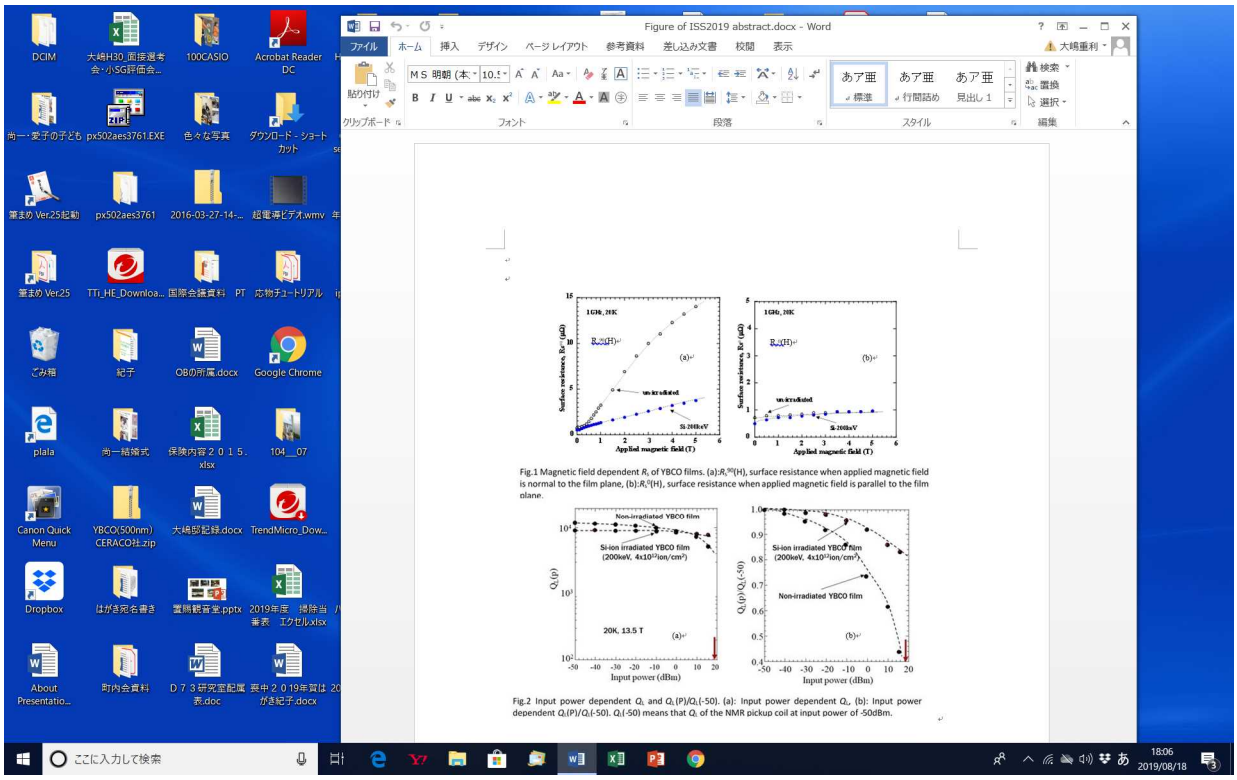
The enhancement sensitivity of the NMR system is roughly classified into the following two methods. One is the development of a high frequency NMR system. Recently, a 1.3 GHz NMR development project has been carried out. The other is to increase the loaded quality factor (Q_L) of the NMR pickup coil. In order to increase the Q_L, it is necessary to reduce the surface resistance (R_s) of the pickup coil materials used under a high magnetic field, and superconducting films are useful for NMR pickup coil materials. We examined the R_s of the Si-ion irradiated YBCO films, and found that the YBCO films irradiated with Si ions have a small R_s [90], and Rs[0] in a high magnetic field (Fig.1). We fabricated the NMR pickup coils using the YBCO films with Si-ion irradiation and without Si-ion irradiation, and found that the NMR pickup coils made with Si ion irradiated YBCO films had large Q_L in high input power region (Fig.2).



Keywords: NMR pickup coil, surface resistance, Si-ion irradiation, YBCO film

EDP1-1

A Study of the HTS Josephson Junction Formed by a Ga Focused Ion Beam

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High Temperature Superconductor Josephson Junctions (HTS-JJs) are based on artificial grain boundaries. However, the layout of HTS Superconducting Quantum Interference Devices (SQUIDs) on a bi-crystal substrate is restricted. Therefore, we explored the use of low noise nano-bridge JJs formed by Ga-Focused Ion Beam (FIB) irradiation.

We have studied properties of HTS films by irradiated Ga-FIB in previous paper [1]. In this paper, we report the fabrication method of HTS nano-bridge JJs and its properties. We deposited 100 nm thick $YBa_2Cu_3O_{7-d}$ (YBCO) films on an MgO substrate by pulsed laser deposition, and 20 nm thick gold thin film as a protection layer was deposited in-situ. After that, we fabricated a 4 μm wide micro-channel by photolithography and an Ar ion milling. Then, we patterned a nano-bridge by FIB irradiation (Acceleration voltage: 40 kV, Beam diameter: ~30 nm, Fluence: 2×10^{15} ions/cm^2) on the micro-channel. As a result, the YBCO layer was normalized leaving a width of 500 nm or 1000 nm as a nano-bridge after FIB process. A SEM image of the typical nano-bridge is shown in Fig.1. The critical current of the 500 nm wide nano-bridge was decreased from 1700 μA to 170 μA at 77 K. The nano-bridge was irradiated by a micro-wave to observe Shapiro steps.

Fig.2 shows the V-I characteristics when the nano-bridge was irradiated by a micro-wave with a frequency f_{RF} of 2 GHz and a power of -13 dBm. A step height of 4.1 μV was observed, consistent with the theoretical value $\Delta V = (h/2e) \times f_{RF}$. This result suggested that the nano-bridge behaved as a Josephson junction. In the future, we plan to apply this fabrication method of the JJ to a low noise SQUID.

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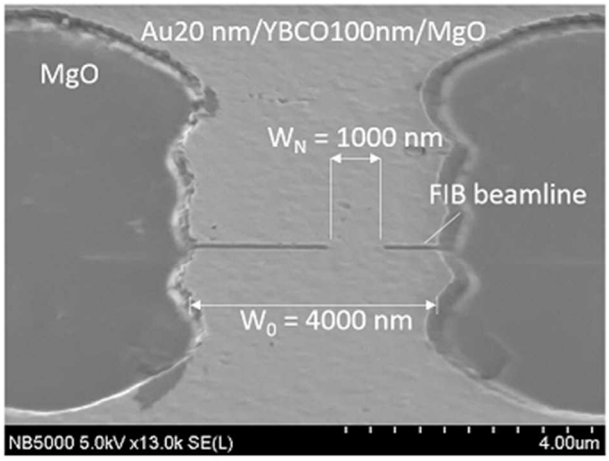

Fig.1 A SEM image of the typical nano-bridge.

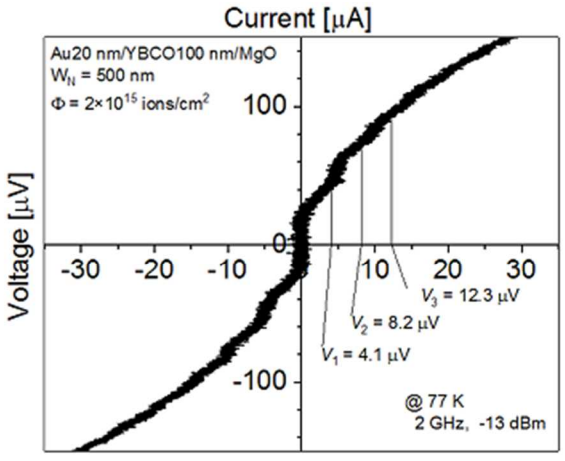

Fig.2 Shapiro-step of the formed nano-bridge.

Keywords: HTS Josephson junction, HTS-SQUID, FIB, Nano-bridge

EDP1-2

Non-contacting ultrasonic guided wave testing for ferromagnetic pipes using HTS-SQUID gradiometer

*Yoshimi Hatsukade[1], Yuki Azuma[1], Keisuke Watanabe[1]

Kindai University[1]

In this work, we investigated non-contacting ultrasonic guided wave testing technique based on magnetostriction method and HTS-SQUID. Magnetization method to transceive T(0, 1) mode guided waves on nickel thin pipe was studied by both electromagnetic field simulator and experiments utilizing magnetostriction method and HTS-SQUID gradiometer. In the both studies, a pair of electromagnets sandwiching a Ni pipe was used to magnetize the pipe, while rotating the pipe between the electromagnets. Both studies demonstrated that the magnetization method enabled us to magnetize the Ni pipe roughly uniformly in the whole circumference and also generate T(0, 1) mode guided waves on the pipe. All-round guided wave testing around the magnetized nickel pipe with artificial defect was also conducted using the HTS-SQUID gradiometer and compared with simulation result using ultrasonic wave simulator. The both results agreed well.

Keywords: HTS-SQUID, T(0, 1) mode ultrasonic guided wave, ferromagnetic pipe, magnetostriction

EDP1-3

Performance of Digital SQUID with Sub-Flux Quantum Feedback Resolution fabricated using 10 kA/cm² Nb process

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The digital SQUID with Single Flux Quantum (SFQ) feedback operates as a delta-type oversampling A/D converter. Magnetic flux resolution at Nyquist frequency can be improved by taking sub SFQ feedback resolution and large oversampling ratio. Using high critical current density Nb process for fabricating SFQ circuits, we expect more higher operation speed of 13 GHz for the digital SQUID and resulting to higher magnetic flux resolutions. In this study, we report on the expected performance of the digital SQUID magnetometer fabricated using 10 kA/cm² Nb process based on CAD layout, with an up/down counter using T²FF cells and parallel SFQ feedback. For the clock frequency of 13 GHz and the Nyquist frequency of 0.793 MHz, the magnetic field noise is lower than 1.5 fT/Hz$^{1/2}$ and the slew rate is exceeded 0.5 T/s. The most promising application of the digital SQUID will be the SQUID transient Electromagnetics (TEM) and these valuses satisfied the requirements.

Acknowledgement

This study has been partially supported by the VLSI Design and Education Center (VDEC) at the University of Tokyo, in collaboration with Cadence Design Systems, Inc. Circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of the National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2) and the high-Jc standard process (HSTP). The AIST-STP2 and HSTP process are based on the Nb circuit fabrication process developed by the International Superconductivity Technology Center (ISTEC).

Keywords: digital SQUID, Single flux quantum circuit, high-Jc Nb process, sub-SFQ feedback

EDP1-4

Implementation of interface circuit for Digital SQUID with sub-Flux Quantum Feedback Resolution

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Digital SQUIDs with the single flux quantum (SFQ) feedback have attracted much attention because of the feasibility of realizing a wide dynamic range and high slew rate for digital magnetometers. In order to realize higher resolution, we have studied a digital SQUID with sub-flux quantum feedback. In this presentation, we will discuss implementation methods for an interface circuit considering circuit size, power consumption and signal processing in order to realize high-resolution and high-speed operation of the digital SQUID magnetometer. Assuming the decimation filter and the up/down counter implemented on a FPGA board, a 1-bit to 16-bit deserializer with output frequency of 500 MHz can be used for interface circuit. This would drastically reduce bias current for the digital SQUID with SFQ feedback operating at 4.2 K.

Acknowledgement

This study has been partially supported by the VLSI Design and Education Center (VDEC) at the University of Tokyo, in collaboration with Cadence Design Systems, Inc. Circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of the National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2) and the high-Jc standard process (HSTP). The AIST-STP2 and HSTP process are based on the Nb circuit fabrication process developed by the International Superconductivity Technology Center (ISTEC).

Keywords: digital SQUID, Single flux quantum (SFQ) circuit, sub-SFQ feedback, digital filter

EDP1-5

Theory for the Response of a Superconducting Kinetic Inductance Detector to an Electromagnetic Wave Packet

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We construct a theory for the response of a superconducting kinetic inductance detector to an electromagnetic (EM) wave packet with a small spatiotemporal extension on the basis of our previous theory for the operation principle of CB-KID [1]. An EM wave packet incident on the superconducting nanowire induces an AC quasi-particle current in the small region where the EM wave packet is irradiated. It is shown that this quasi-particle current generates voltage pulses inductively, which propagate towards both ends of the superconducting nanowire. In the current-biased case the kinetic inductance of the detector is also varied by a hot spot originating from the damping of the quasi-particle current. As a result, a pair of voltage pulses with opposite polarities are generated. The possibility to detect single-photons in this detector is also discussed.

Keywords: kinetic inductance detector, superconducting nanowire

EDP1-6

Reduction of the leakage current for embedded STJ

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Superconducting tunnel junction (STJ) is expected as a next-generation photon detector because of high energy resolution, high counting rate and wide energy range. However, the detection area of single STJ is limited to 0.01 mm^2. One of the solutions is the expansion of the detection area by the array of the STJ. The conventional array format of the STJ also has a problem. Large format arrays will reduce the detection efficiency because of its larger number of the contact wires. To solve this problem, we have proposed an embedded STJ (e-STJ) with through Si via as shown in Fig. 1 (a). The detection efficiency of the e-STJ is not affected by the number of the wires. A simple e-STJ in Fig. 1(b) has shown good I-V characteristic at 4.2 K.
So far, the I-V characteristics of the simple e-STJ showed large leakage current at 0.3 K. In this research, we fabricated a conventional STJ and three types of e-STJ : simple e-STJ and e-STJ where the side surface of the STJ is not in contact with the Si substrate and e-STJ where only the side surface of the base electrode layer is in contact with the Si substrate. Then, the cause of the large leakage current at 0.3 K was investigated. We will present about the fabrication methods and the experimental results.

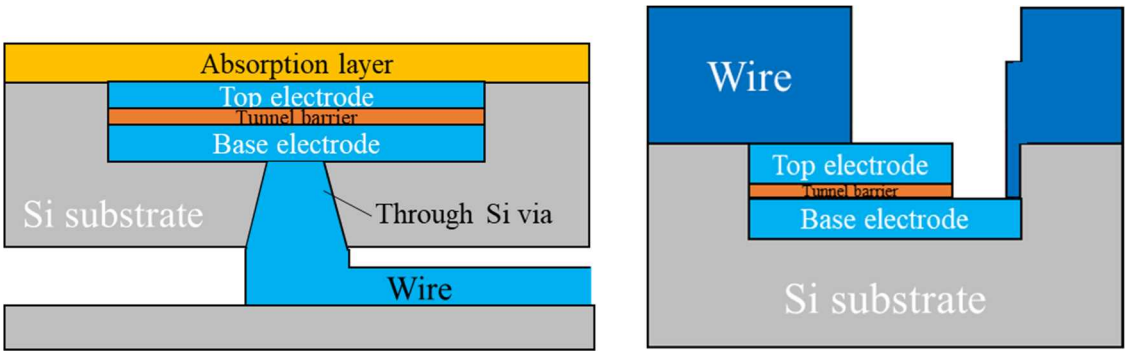

Fig.1 (a) Cross view of e-STJ with through Si via and (b) Cross view of a simple e-STJ

[1] T. Ishizuka et al., The 74th Japan Society of Applied Physics Autumn Meeting, 17p-C10-20 (2013).

EDP1-7

Improvement of spatial resolution using Substrate Absorption type STJ

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An electromagnetic wave having a frequency range from 0.1 to 10 THz is called a THz (terahertz) wave. It is expected to find applications in various fields since it has both radio wave and light wave. We have proposed a substrate absorption type superconducting tunnel junction (STJ) for the THz detector that absorbs the THz waves by the substrate and detects phonons generated in the substrate [1].

The phonon isotropically diffuses in the substrate when the THz waves are illuminated from the opposite side of the STJ across the substrate. It causes the degradation of the spatial resolution. To solve this problem, we have proposed a new THz detector which restricts the phonon diffusion by trenches on the back side of the substrate as shown in Fig 1. The trenches have Al layer which prevents the absorption of the THz wave at the trenches. The formation of the trenches and the deposition of the Al layer do not affect the quality of the STJ [2]. In this research, we demonstrate the phonon restriction using the trenches. The fabrication method and the measured results will be presented.

[1] C. Otani *et al.*, IEEE Trans. Appl. Supercond., Vol. 15, No. 2, pp. 591- 594 (2005).
[2] M. Sone *et al.*, Journal of Physics: Conf. Series, 871, 012069 (2017).

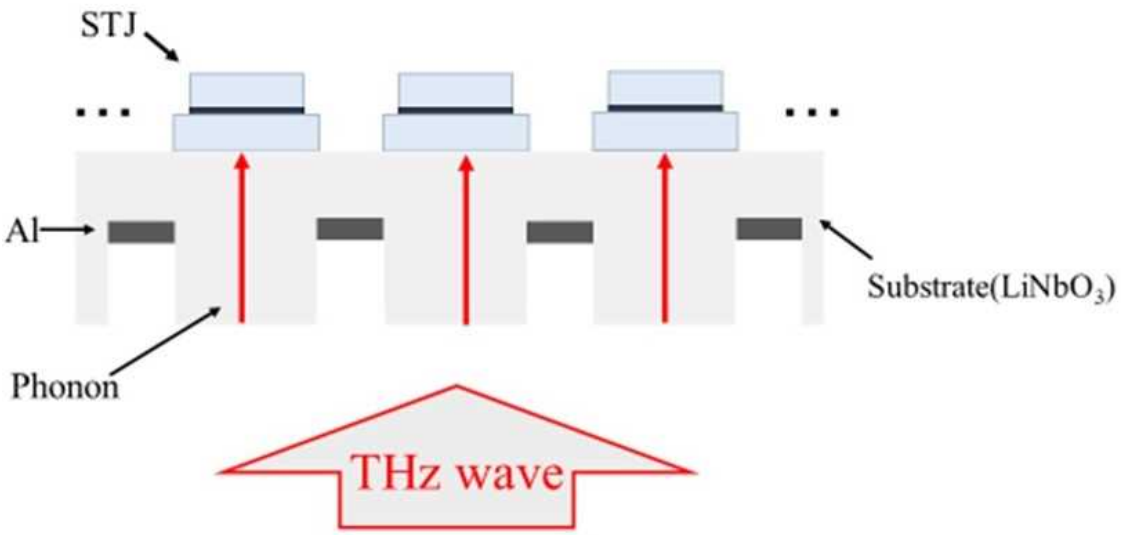

Figure 1. A schematic view of our proposed STJ

Keywords: Superconducting tunnel junctions, Terahertz wave

EDP1-8

Develipment of STJ with large detection area for neutron detector

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Since neutron is permeable to metals and sensitive to light elements such as hydrogen, lithium and boron, it can nondestructively evaluate a bulk texture of metallic materials. Therefore, it has been expected as a new imaging tool in the industrial fields such as automobile industry and construction industry and so on. However, conventional neutron detectors can realize indeed a large sensitive area (> cm^2), but they only have poor spatial resolution of the order of millimeters. On the other hand, superconducting tunnel junctions (STJs) on a single crystal $Li_2B_4O_7$ (LBO) substrate have proposed as a next generation neutron detector because of its high detection efficiency [1]. In case of STJs, a high spatial resolution (< 50 mm) can be possible but it is fairly difficult to satisfy the required sensitive area (10 cm × 10 cm) of the detector for industrial applications, because the area of single STJ is limited to 0.1 mm × 0.1 mm due to its own characteristics and then at least 1 million pixels are necessary to cover the whole required sensitive area, which leads to a quite large heat load to cryostats through 2 million wires. That is not realistic. Therefore, it is necessary to introduce another approach for realizing such a large sensitive area and a high spatial resolution, simultaneously.
In this research, we proposed and fabricated a new substrate absorption type STJ for neutron detection with 1 pixel size of 5 mm × 5 mm, which can be expected to achieve large detection area by using a small number of STJs. Fig. 1 shows our proposed neutron detector. Neutron is irradiated from the substrate. 4 STJs detect phonons generated in the substrate by nuclear reactions of neutron with Li and B. Theoretically, the position of the neutron absorption can be determined precisely from the each pulse height of STJ[2]. The geometric configuration of STJs should be decided to realize a high special resolution as well as a large detection area. In order to determine the above configuration, it is necessary to evaluate the phonon diffusion length in the substrate. As a first step, we have tried STJs on LBO substrates and determined the phonon diffusion length to design the appropriate neutron detector based on STJs. The fabrication method and the evaluation results will be presented.

[1]T.Nakamura et al., Nucl. Instr. and Meth.,m A 529, 402-404 (2004).
[2]H.Kraus et al., Phys Lett. B 231, 195 (1989).

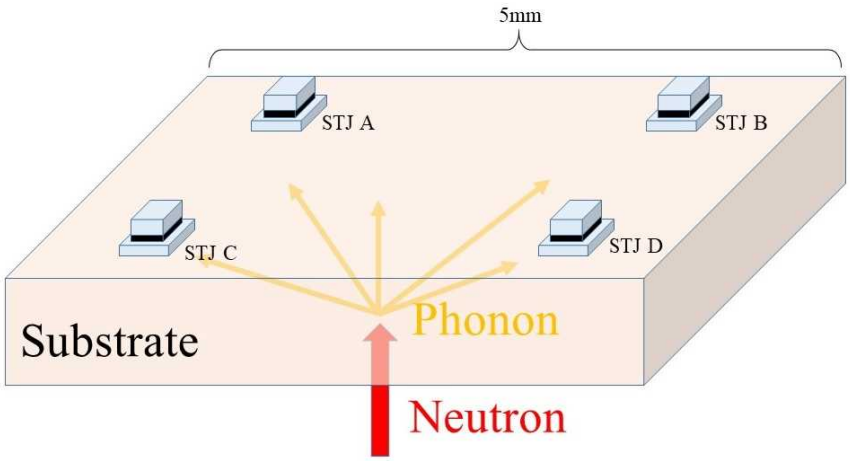

Fig.1 Our proposed neutron detector

Keywords: Superconducting Tunnel Junction, Neutron detector

EDP1-9

Development of Superconducting Single-Photon Detector(SSPD) using molybdenum nitride thin film

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In recent years, there is an increasing demand for high-performance single photon detectors in a wide range of research fields including quantum information communication and quantum optics. Among them, SSPD is a detector having a single photon sensitivity from the ultraviolet region to the mid-infrared region (0.3 μm to 0.5 μm). Furthermore, its excellent performance of high sensitivity and high speed response is expected to be applied to future communications. The superconducting material used greatly affects the detector performance. Currently, niobium nitride (NbN) is often used as a superconducting material for SSPD. However, this study focused on molybdenum nitride (MoN) as a new material. The reason is that MoN has a maximum Tc slightly lower than NbN, but has an electron-lattice relaxation time that is one order of magnitude longer. As a result, a detector with higher internal detection efficiency than that using NbN is obtained. Furthermore, we succeeded in developing the SSPD using MoN with high system detection efficiency by adding a cavity structure and an anti-reflection coating layer.
This work is supported in part by JSPS KAKENHI 18K04255 and by the Cooperative Research Program of “NJRC Mater. & Dev.”.

Keywords: SSPD, MoN

EDP1-10

Improvement of detection efficiency by reducing shunt resistance of SSPDs

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Superconducting single-photon detectors (SSPDs) are based on nano-scaled width strips. This is because it has been empirically known that SSPDs can't detect single-photons with the wider strips. Even if it's possible, the detection efficiency is low. Recently, it has been reported that when a bias current (I_{bias}) is applied close to the depairing current (I_{dep}), it can detect single-photons even with the micron-scaled bridges [1]. Here, we report our results using the micron-scaled bridges as well as the nano-scaled stripes with various shunt resistances (R_{sh}). We found that the single-photon detection is possible even with a micron-scaled bridges by applying R_{sh}, and the system detection efficiency (η_S) of the micron-scaled bridges increases by reducing R_{sh}. We also report the improvement of η_S with nano-scaled strips by further reducing R_{sh}.
This work is supported in part by JSPS KAKENHI 18K04255 and by The Telecommunications Advancement Foundation.
References
[1] Y. Korneeva et al. Phys. Rev. Appl. 9, 064037 (2018).

Keywords: SSPD, SNSPD, shunt resistor

EDP1-11

Iridium-based superconducting optical transition edge sensor for single-photon detection

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Optical quantum imaging or information processing is expected to be a new technology to surpass classical noise and resolution limit by fully exploiting the characteristics of non-classical photon sources. In such applications, photon-number resolving capability and high detection efficiency is required for the photon detector. The superconducting transition edge sensor (TES) is the ideal detector for this application, since it has the nearly 100 % detection efficiency with optical cavity structure and the almost linear response to simultaneously absorbed multi-photons. A TES consists of a superconducting thin film which is biased with a constant voltage. When optical photons are absorbed in the film, the photon energies are transformed into a very small increase of temperature in the film and hence the increase of its resistance, causing small current signal which is measurable with superconducting quantum interference device (SQUID).

To enhance the energy resolution of optical TES and hence its photon number resolving capability in near infrared regions, we are developing optical TES based on single-layer iridium film by exploiting its very low transition temperature (140 mK in bulk). We fabricated optical TES with iridium film with the minimum size of $7 \times 7\ \mu m^2$. The iridium film was deposited on SiN/Si/SiN substrate, and Nb contact electrodes were formed. We confirmed the response to optical photons in near infrared wavelengths (860 nm and 1310 nm) using iridium optical TESs. The design of optical cavity structure for iridium TES is ongoing, and its performance will be discussed too.

EDP1-12

Kinetic inductance neutron detector operated at near critical temperature

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Superconducting detectors have the advantages of high sensitivity, fast response, and high energy resolution such as a transition edge sensor [1], a superconducting nanowire single-photon detector [2], and a microwave kinetic inductance detector [3]. We first proposed a superconducting neutron detector using an MgB_2 superconductor [4]. Later on, we extended the idea to a current-biased kinetic inductance detector (CB-KID) [5] which consists of two orthogonal superconducting Nb meanderlines with a ^{10}B neutron conversion layer. The CB-KID neutron imager detects high spatial resolution neutrons transmission images by using a delay-line technique. We reported a spatial resolution of 22 μm [6]. The physical characteristics of a CB-KID detector have been studied systematically [7,8]. The theoretical basis of CB-KID was studied by means of the Maxwell-London theory [9]. Prior to this study, we found that the number of events was remarkably increased with increasing the detector temperature until close to the critical temperature Tc [10]. In the present study, we investigated the properties of CB-KID at near T_c.

We observed systematic changes of neutron signals as a function of the detector temperature from 4 K to T_c.

We evaluated the detection efficiency of the CB-KID detector and compared with PHITS Monte Carlo simulations. The simulations modeled the sequential physical processes for 10B(n,α)7Li reactions and energy deposition by particles within CB-KID, including neutrons, ^{4}He particles, ^{7}Li particles, photon and electron transport [11].

This work was partially supported by a Grant-in-Aid from the Japan Society for the Promotion of Science (JSPS) (No. 16H02450).

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Keywords: Superconducting detector, neutron detector, CB-KID, pulsed neutron

EDP1-13

Design and fabrication of Programmable Josephson Voltage Standard Circuit for 100 V ac-voltage standard

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The Programmable Voltage Standard (PJVS) Circuit having the output voltage of 32 V has been designed and fabricated for ac voltage standard. While our PJVS chip for primary dc voltage standard at NMIJ has the maximum output voltage of about 16 V, the voltage for commercial power in Japan is 100 Vrms and 141 Vpp.
We plan to generate 141 Vpp by combining 5 chips of 32 V PJVS circuit.
Thus, twice higher integration density of Josephson junction and the uniform power distribution for them are necessary to generate such high out put voltage with practical operating margin.

To integrate a million of Josephson junctions on the 15 mm x 15 mm chip, the junction size has been changed from 3.4 um x 3.4 um to 1.2 um x 4.0 um.
Although vertically stacked double barrier Josephson junctions are used to integrate such large number of Josephson junctions, the poor uniformity of the critical current between the upper and lower junction significantly decreased the Shapiro step height. We have found that the grain sizes of the barrier layer of TiN film for the upper junction is larger than that for the lower junction. The surface flatness of the NbN film nearly proportional to the thickness.

We experimentally confirmed that the critical current of the NbN/TiN/NbN Josephson junction depends on the thickness of the base electrode.
This suggests that the difference of the critical current between the upper and lower junction caused from the difference of the crystalline nature such as grain size of the barrier TiN. The lower Josephson junction has smaller critical current and the upper Josephson junction has higher one. And this provides a clue to improve the uniformity of the critical currents between the lower and upper junction, which may significantly increase integration density for Josephson junctions.

Keywords: ac voltage standard, double barrier Josephson junction, NbN, grain size

EDP1-14

Optical Ppulse-Driven Integrated Quantum Voltage Noise Source for Johnson Noise Thermometer

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We have developed an integrated quantum voltage noise source (IQVNS) as a reference signal source for the Johnson noise thermometer. The Josephson effect ensures that the power spectral density of the output signal of IQVNS is described by a combination of Planck's constant h, elementary electric charge e, clock frequency of IQVNS f_c, and numerical coefficient. One of the features of IQVNS is that it has a random number generator on the superconducting device. Therefore, it is not necessary for IQVNS to use a pulse pattern generator that can be an unwanted electrical noise source for the Johnson noise thermometer. However, IQVNS is coupled with a microwave oscillator for supplying a clock signal using a metallic coaxial cable, and there is still a possibility of picking up unwanted noise signals.
In this study, we tried to eliminate the metallic wiring to IQVNS completely by using optical pulse as clock signal to IQVNS. The light pulse transmitted through the optical fiber is converted into a current pulse by a photodiode mounted on the IQVNS probe head. Using this optical pulse driven IQVNS, the thermal noise of the resistor placed at the triple point of water was measured, and the temperature of the triple point of water was derived.

Keywords: Johnson noise thermometry, quantum voltage noise source, rapid single flux quantum circuit, Optical pulse

EDP1-15

Investigation of Thermal Resistance in a Cryopackage for Programmable Josephson Voltage Standard Device

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Since 2016, a programmable Josephson voltage standard (PJVS) system based on a liquid-helium-free cryocooler has been in practical use at NMIJ. In this system, however, there is a problem that the chip temperature slightly rises with the output voltage level, narrowing the bias-current margin for the PJVS device operation.

In our previous study, it was found that many voids existed in the solder layer used in our cryopackage and might be one of the possible causes for the temperature rise in the PJVS chip [1]. We investigated the void-ratio dependence of the thermal resistance both in the numerical simulations and the experimental measurements, and showed that the thermal resistance rapidly increases with the void ratio of greater than 80 %.

In this study, we are investigating more details of the void-ratio dependence and other measurements for the thermal resistance of our cryopackage for the PJVS device. Up to now, we found that the obtained data for the void-ratio dependence cannot be fitted by the simulated dependence, indicating the existence of a large residual thermal resistance of the order of 1 K/W or more (Fig. 1). We are now trying to reveal the cause for such the large thermal resistance.

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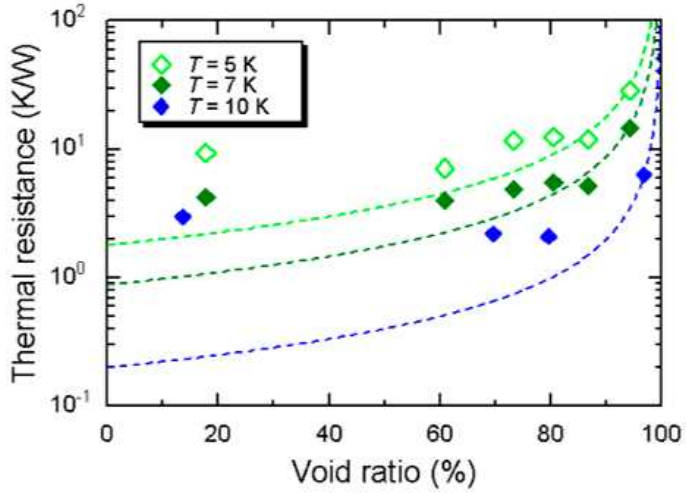

Fig. 1 Measured thermal resistances of the cryopackage for the PJVS device versus the void ratio in the solder layer. The broken lines indicate the fitting lines based on a simulation.

Keywords: Cryopackage, Josephson voltage standard, PJVS, Thermal resistance

EDP1-16

Estimation of Electricity Storage Density of Compact SMESs Composed of Si-wafer Stacks Loaded with Superconducting Thin Film Coils in Spiral Trenches under the Constraint of Critical Magnetic Flux Density

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We have been developing a superconducting thin film coil in a spiral trench on a Si wafer [1]. Having completed in fabrication of a NbN superconducting thin film coil on 76.2 mm-diameter Si wafer [2], we have replaced NbN with $YBa_2Cu_3O_{7-\delta}$[3]. The high critical current density of $YBa_2Cu_3O_{7-\delta}$ is possible to impose high magnetic flux density as well as electromagnetic hoop stress on the coil. In the constraint of the upper limit of critical magnetic flux density of 20 T for $YBa_2Cu_3O_{7-\delta}$ and hoop stress of one third of 4 GPa for Si wafer, the design of the spiral coil must be optimized. For this purpose, estimation of magnetic field generated by the superconducting current in the spiral coil was performed based on Biot-Savart low [4]. The spiral coil was approximated to be multiple loops with the same current in a 101.6 mm Si wafer and 600 wafers were supposed to be stacked. The sum of the generated magnetic fields was obtained at the innermost loop in the trench to obtain the maximum magnetic flux density and hoop stress in the 600 wafers. A typical result in Figure 1 shows the maximum electricity storage density of 13.8 Wh/*l* appeared at the innermost coil radius about 45.4 mm. The hoop stresses were well below the one third of 4 GPa.

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[2] Suzuki N et al., **2017,** IOP Conf. Series: Journal of Physics: Conf. Series 897, 012019
[3] Ichiki Y et al., 2018, IOP Conf. Series: Journal of Physics: Conf. Series 1054, 012065
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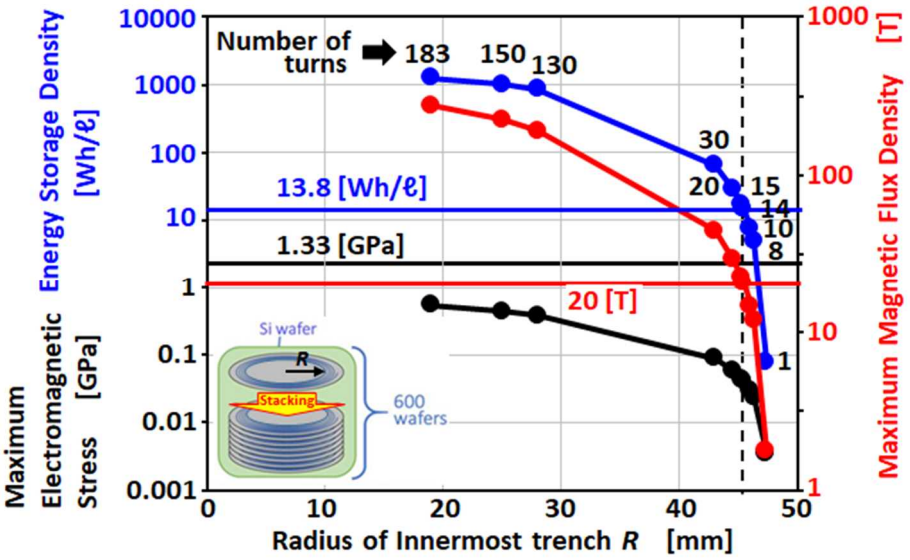

Fig. **1** A typical result of estimations of energy storage, maximum magnetic flux density and maximum electromagnetic stress as a function of the radius of the innermost trench radius.

Keywords: Electricity storage density, SMES, Si wafer, Critical magnetic field

EDP1-17

Evaluation of surface morphology of Pb-In alloy films for superconducting bumps utilized in a three-dimensional packaging structure of X-ray detector

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Superconducting tunnel junction (STJ) is one of the candidates as an x-ray detector because of high energy resolution. In order to obtain a two-dimensional image of detected x-ray, it is necessary to array a large number of STJs on a chip. However, the integration density of STJs is limited by the wiring area when the STJ-array is enlarged. To solve this problem, we have proposed an "embedded STJ" (e-STJ) with a three-dimensional packaging structure [1].

A Pb-In alloy bump is one candidate for using the superconducting connections in the three-dimensional packaging structure. We found some roughness on the bump surface in the previous research. In order to realize multi-pin connection technology, it is necessary to flatten bump surface to reduce bonding force. Thus, we investigated the surface of superconducting Pb-In alloy bumps to clarify the effect of surface morphology on the superconducting Flip-chip Bonding (FCB) connection.

A Pb and In films were deposited on an oxidized Si wafer by evaporation sequentially to make Pb-In stacking films with various mass concentration of In in Pb. Total thickness of the stacking film was made to be 4 μm. The calculated average roughness (Ra) and the maximum height (Rz) of Pb-In stacking film surfaces were measured at room temperature after annealing time of over 100 hours for alloying. Ra and Rz of the Pb-In stacking films are plotted as a function of the mass concentration of In in Pb in Fig. (a) and (b), respectively. The roughness of Pb-In stacking film surfaces increased after alloying than the pure Pb and In films as shown in the figures. The details will be presented.

[1] T. Ishizuka et al., 74th the Japan Society of Applied Physics, 17 p-C10-20 (2013).

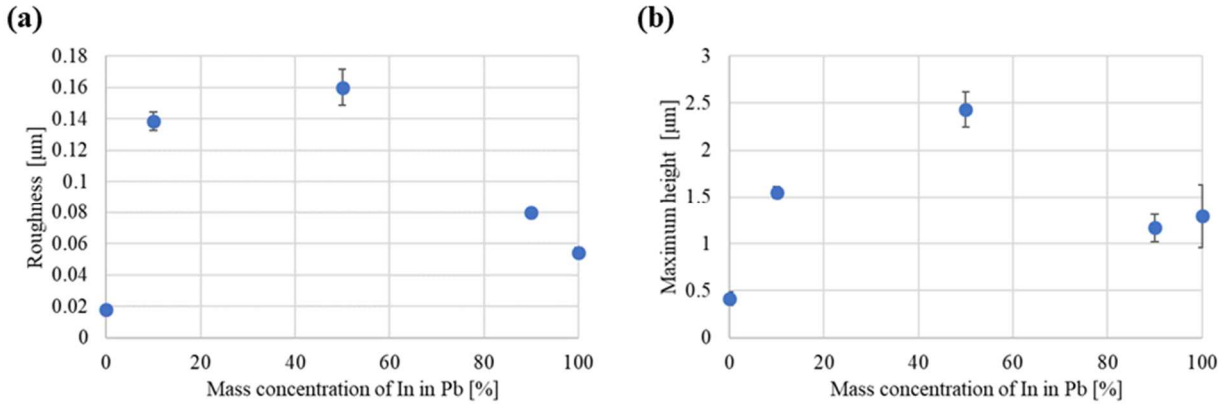

Fig.(a) Ra of Pb-In stacking film surface (b) Rz of Pb-In stacking film surface

Keywords: Superconducting tunnel junctions, Flip-chip bonding, Bump

EDP1-18

Micro-Fabrication of NdFeAs(O,F) Thin Films and Evaluation of the Transport Properties for Future Particle-Detector Application

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Photon and ion detectors based on superconducting nanowires have been attracting substantial attention because they are superior to conventional detectors in terms of high-speed operation, high sensitivity, and low noise characteristics. To realize these excellent performance, the superconductor has to be fabricated into narrow wires with a width of about 300 nm for an ion detector and 100 nm or less for a photon detector. Detectors based on conventional BCS superconductors such as Nb and NbN have been already extensively studied [1]. However, the operating temperature is low due to their low transition temperature (T_c). As for the high-T_c superconductors, there are several attempts to fabricate detectors from MgB_2 and copper-oxides [2-4], yet they suffer from a notable degradation of the superconducting characteristics when the wires become narrow. On the other hand, little is known about the performance of nanowires based on iron-based superconductors. In this work, we fabricated narrow wires from thin films of NdFeAs(O,F), which has the highest T_c (= 56 K) among iron-based superconductors, and evaluated their transport properties.

High-quality single crystalline thin films of NdFeAs(O,F) were grown on MgO substrates by a molecular beam epitaxy method [5]. The film was patterned into a two-island structure connected by a narrow wire (40-nm-thick x 0.35-μm-wide x 10-μm-long) using i-line lithography and Ar ion milling. The as-grown film exhibited a zero T_c of 40 K, whereas the fabricated wire still kept T_c = 38 K as displayed in Fig. (a). The critical current density (J_c) was 1.3 MA/cm^2 at 4 K as shown in Fig. (b). These results indicate that degradation of the superconducting properties of NdFeAs(O,F) due to nano-processing might not be as serious as other high-T_c superconductors.

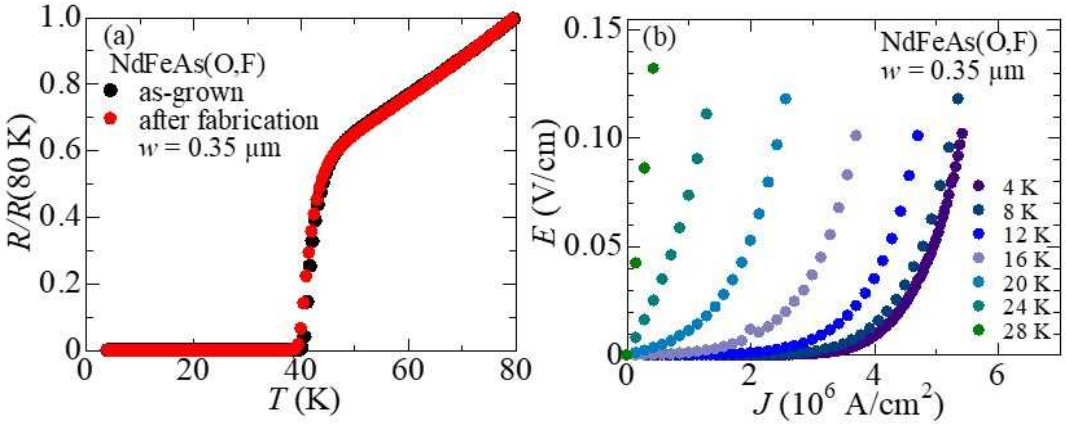

Fig. (a) Temperature dependence of the resistivity, and **(b)** current density (J) dependence of the electric field (E) of the fabricated wire. The data of the as-grown film are also shown in (a).

[1] C. M. Natarajan *et al.*, *Supercond. Sci. Technol.* **25**, 063001 (2012). [2] H. Shibata *et al.*, *Appl. Phys. Lett.* **97**, 212504 (2010). [3] N. Zen *et al.*, *Appl. Phys. Lett.* **106**, 222601 (2015). [4] R. Arpaia *et al.*, *Phys. Rev. B* **96**, 064525 (2017). [5] T. Kawaguchi *et al.*, *Appl. Phys. Lett.* **97**, 042509 (2010). T. Kawaguchi *et al.*, *Appl. Phys. Express.* **4**, 083102 (2011).

Keywords: Micro-fabrication, Epitaxial thin film, Iron-based superconductor, Particle detector

EDP1-19

Prototyping new type $Bi_2Sr_2CaCu_2O_{8+x}$ devices using a consumer-oriented inkjet printer

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We are attempting to prepare planar type intrinsic Josephson oscillator devices. These new type devices can be prepared by a combination of orientation control technique of $Bi_2Sr_2CaCu_2O_{8+x}$ (Bi2212) thin film by solution method and printing method using inkjet printer. In order to prepare these planar type devices, it is necessary to form a current path parallel to the substrate, so that the *c*-axis of Bi2212 is required to be parallel to the substrate.

We have prepared (010) (or (100)) oriented Bi2212 thin films by metal-organic decomposition (MOD) method which is one kind of solution method [1]. When using vicinal (100) substrates, the Bi2212 (020) (or (200)) peak appeared clearly in the X-ray diffraction patterns. From the scanning electron microscope (SEM) image, it was found that elongated plate-like crystal grains of Bi2212 were grown. From the viewpoint of lattice matching, this elongated crystal grain is considered to be (010) (or (100)) oriented Bi2212 crystal grains.

Since we have succeeded in forming crystal grains that the *c*-axis is parallel to the substrate, we are now attempting on prototyping device using a consumer-oriented inkjet printer. The main component of the solvent in the Bi2212 raw material solution is xylene. Some inkjet printer components have low resistance to xylene, such as the packing of the printer head. Therefore, the Bi2212 raw material solution cannot be used by filling in the ink cartridge. In this report, microfabrication is performed by lithography and chemical etching. The printing method using an inkjet printer is applied to the lithography process. The device fabrication procedure is as follows.

(1) Using a spin coater, the raw material solution is applied to the entire surface of the substrate.
(2) The substrate coated with the solution is heat-treated using an electric furnace.
(3) Photoresist is applied to the sample in a desired pattern using an inkjet printer.
(4) Etching with acid is performed.
(5) The photoresist is removed.

We are using an EPSON inkjet printer capable of CD label printing. The samples will be evaluated based on SEM images and electrical characteristics. Details will be discussed in the presentation.

[1] Yamada Y et al., Journal of Physics: Conference Series (to be published)

Acknowledgments: This work was supported by JSPS KAKENHI Grant Number JP17K06377.

Keywords: BSCCO, metal-organic decomposition method, orientation control, printing method

EDP1-20

Design of High Quality Factor RF Coil Using Superconducting Bulk

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University of Yamanashi[1]

It is main problem that improvement of the power transfer efficiency of Wireless Power Transfer (WPT) system. The power transfer efficiency depends on the quality factors of the transmitting and receiving coils. However, it is difficult to improve the quality factors of them due to the limitation of conductivity of the normal conductor such as copper used for the coils. To overcome this problem, we designed a high-quality factor coil using the superconducting bulk. Figure 1(a) shows the structure of superconducting bulk simulated with 3D electromagnetic simulator. Figure 1(b) shows the quality factor of the coil versus the gap between lines with each line width. The resonant frequency is 40 MHz. The quality factor of the superconducting bulk coil is 30 times higher than that of the copper coil when gap between lines and line width are 1.5 mm and 1.5 mm.

We also simulated the coil quality factor with dielectric supporting material because the superconducting bulk coil can't maintain the spiral coil structure without it. We will show the detail of the preliminary experiments using superconducting bulk coil at the conference.

Acknowledgment: This research and development work was supported by the MIC/SCOPE #181603014.

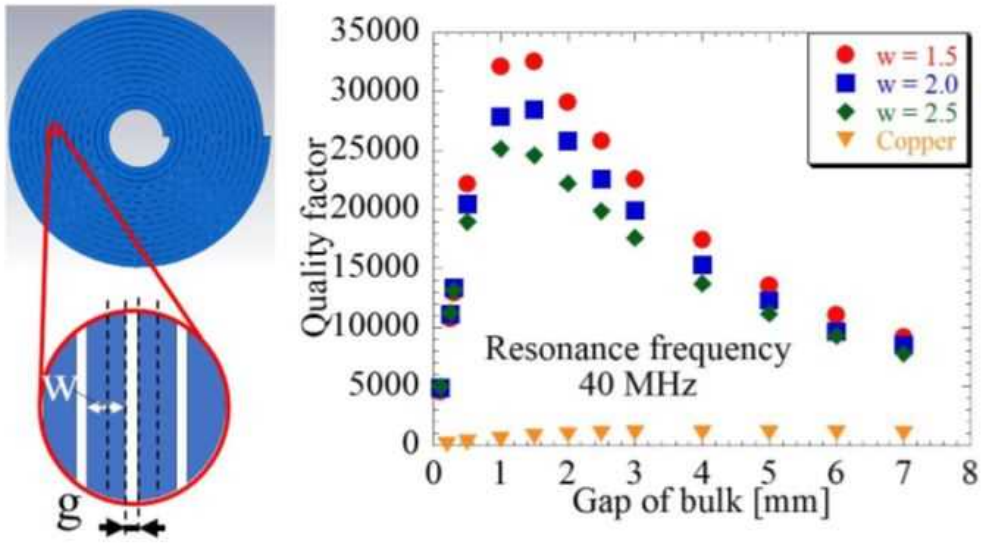

Figure 1. (a) Structure of superconducting bulk coil,
(b) Quality factor dependences on gap between lines with each line width

Keywords: Wireless Power Transfer (WPT), Superconducting bulk coil, RF coil, Quality factor

EDP1-21

Development of Superconducting Filter for Deep Space Exploration Ground Station Receiving System

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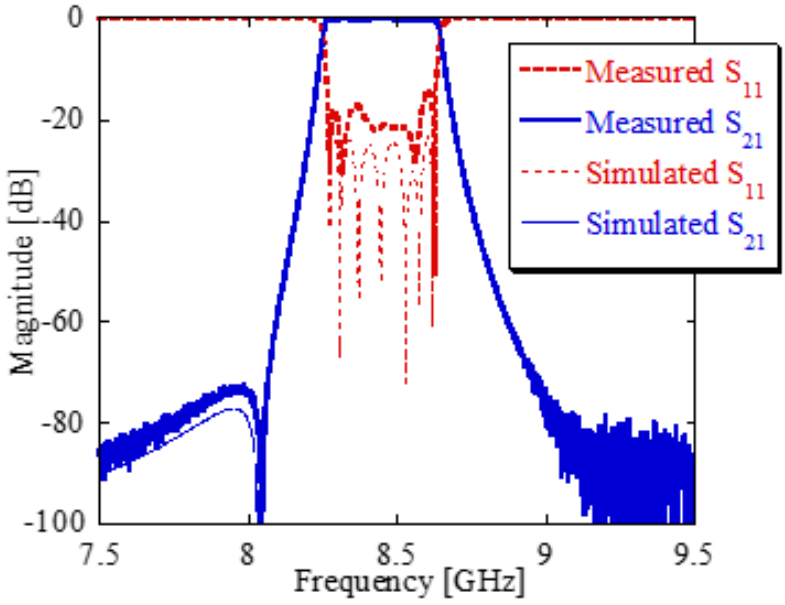
We have developed a superconducting filter for deep space exploration receiving system. JAXA (Japan Aerospace eXploration Agency) is currently developing new antenna for deep space exploration. New antenna requires high performance filter which has compact size, low insertion loss and high selectivity. In this study, we developed a superconducting filter which satisfied these requirements and design specification accurately. The filter was fabricated using $YBa_2Cu_3O_7$ thin film on r-Al_2O_3 substrate. An r-Al_2O_3 substrate has strong mechanical strength, high chemical stability and low cost. However, there is the problem that it is difficult to agree well with the simulated and measured result, because of dielectric anisotropy, so that there is no practical superconducting filter using r-Al_2O_3 substrate. Therefore, we proposed the design method which consider dielectric anisotropy of the substrate. In addition, to improve the degradation of the frequency response due to the discrepancy of the substrate thickness and dielectric constant difference between design and fabrication we used dielectric rods. Figure 1 shows the simulated and measured frequency responses of the filter. The measured results agree well with the simulated ones. We used the dielectric rods to reduce the return loss. Finally, our filter was adopted for the receiving system of the JAXA Ground Station for Deep Space Exploration and Telecommunication (GREAT).

Acknowledgment
This work was executed in the development of low noise amplifier equipment for JAXA GREAT project.
We would like to thank the member of GREAT project team.



EDP2-1

Design and Error-Rate Evaluation of RSFQ Logic Gates Comprising a Toggle Storage Loop

*Koki Yamazaki[1], Hiroshi Shimada[1], Yoshinao Mizugaki[1]

The University of Electro-Communications[1]

RSFQ circuits are being investigated for microprocessor applications that take advantage of high-speed switching and low power consumption [1]. As the RSFQ circuit becomes larger, problems such as the complicated clock wiring, the increased bias current, and the increased magnetic field in the circuit adversely affect the circuit operation. Therefore, a simpler configuration is preferable for RSFQ logic cells. We have designed an area-reduced NOT-gate, in which a toggle storage loop is employed, for the purpose of reduction of these problems. Besides, bit error rate(BER) is another important indicator of the quality of digital transmission systems. In this paper, we evaluate the operation and BER of logic circuits including our area-reduced NOT gate.

The equivalent circuit of the area-reduced NOT gate is shown in fig. (a). Its NOT operation is as follows. When an SFQ is fed from the set terminal, J3 is switched to hold the SFQ in the J3-J4 storage loop. After another SFQ comes from the clock terminal, J4 is switched and the held SFQ is annihilated, which means no SFQ at the output terminal. When an SFQ is fed from the clock terminal without an SFQ in the J3-J4 storage loop, J6 is switched and the SFQ goes to the output terminal.

Test chips were fabricated using the Nb 2.5kA/cm^2 process(STP2) at the National Institute of Advanced Industrial Science and Technology(AIST), Japan.

The measurement was performed in a liquid helium bath. Fig. (b) shows the bias current versus BER for the 2.4×10^5 input of "0" and "1". No errors were observed for the bias current between 12.48mA and 13.71mA. Experimental results were fitted well with complementary error functions except for 2 points.

[1] e.g., Y. Ando, et. al., IEEE Trans. Appl. Supercond., **26**, (2016) 1301205.

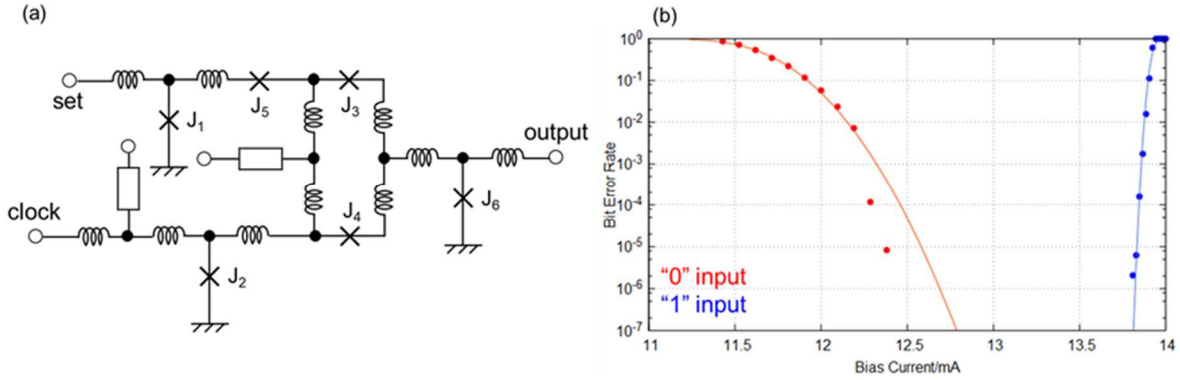


Fig. (a): Equivalent circuit of the are-reduced NOT-gate. (b): Experimental result and fitting curves of BER for the inputs of 2.4×10^5 "0" and "1"

Keywords: Nb integrated circuit, Bit-Error-Rate, RSFQ digital circuit

EDP2-2

Single-Flux-Quantum Parallel Multiplier Using Accumulator Unit

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A multiplier is one of fundamental circuit elements for digital circuits. So far, single-flux-quantum (SFQ) multipliers based on various hardware algorithms have been investigated. Conventional SFQ multipliers required relatively large circuit areas because the adder tree is used to sum partial products. In this study, we investigated and designed a new SFQ parallel multiplier that uses a parallel accumulator unit. Because the accumulator unit, which is composed of resettable toggle flip-flops, can be used as the parallel counter, the circuit area for summation of partial products can be drastically reduced. We designed and simulated a 4-bit SFQ parallel multiplier based on the investigated hardware algorithm using the AIST 10 kA/cm^2 Nb advanced process. The target operating frequency is 30 GHz. The multiplier can be used as a multiplier-accumulator (MAC). Thought the operating frequency of the designed multiplier is slightly lower than that of the conventional SFQ parallel multiplier, the circuit area can be reduced. The number of Josephson junction to implement 4-bit multiplier is 1374, which is approximately half of that of the conventional 4-bit SFQ parallel multiplier.

Acknowledgment
This work was supported by JSPS KAKENHI Grant Number JP 18K04280. The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the advanced process 2 (ADP2).

Keywords: SFQ circuits, multiplier, accumulator, adder;MAC

EDP2-3

Investigation of influence by flux trapping for interconnection of adiabatic quantum-flux-parametron circuits

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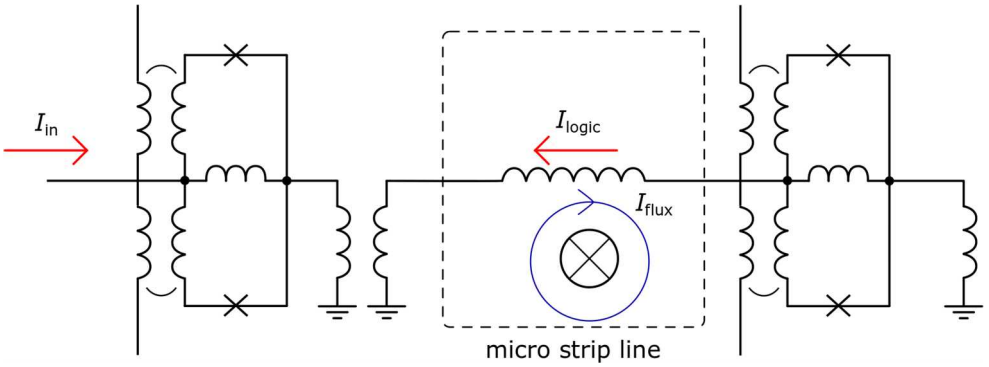
Institute of Advanced Sciences, Yokohama National University[2]

Adiabatic quantum-flux-parametron (AQFP) logic is known as an energy efficient superconductor digital logic family [1]. When compared to the state-of the-art CMOS technology, AQFP has a high advantage in term of power consumption. To realize large scale AQFP integrated circuit, many studies are ongoing [2][3].
One problem that has recently emerged is low yield of circuits with complex interconnect. One possible cause is magnetic flux trapping. A trapped magnetic flux is a physical phenomenon that occurs mainly in the ground layer. When a normal conduction region is surrounded by a superconducting one, permanent current flows around that region. The current and magnetic flux are thought to affect the circuit and cause malfunctions.
The logic state of an AQFP circuit is encoded as the direction of current, and each AQFP gate are connected by a superconducting stripline. The amplitude of the data signal current maybe smaller than the circular current that is generated by the trapped flux, especially for long, complex interconnect whose large parasitic inductance already attenuates the AQFP current output. Therefore, circuit malfunctions may happen as the data current signal is negatively influenced by trapped flux along the interconnect, resulting in the incorrect sampling of data in the receiving AQFP gate.
It is very difficult to completely avoid magnetic flux trapping. One solution is adapting moats along the interconnection. Moats are done by creating slits in the ground plane, and by creating defects such that trapped flux are guided to the moat [4]. In this time, we designed a test circuit with the application of various moat structures and considered its effectiveness in AQFP circuits.

[1] Takeuchi, N., Ehara, K., Inoue, K., Yamanashi, Y., & Yoshikawa, N., IEEE Transactions on Applied Superconductivity, 23(3), 1700304–1700304 (2013).
[2] Yamae, T., Takeuchi, N. & Yoshikawa, N., Supercond. Sci. Technol. 32, 035005 (2019).
[3] Cai, R. et al., in Proceedings of the 46th International Symposium on Computer Architecture 567–578 (ACM, 2019).
[4] Polyakov, Y., Narayana, S. & Semenov, V. K., IEEE Trans. Appl. Supercond. 17, 520–525 (2007).



Keywords: Superconducting integrated circuit, Adiabatic Quantum Flux Prametron, Flux Trapping

EDP2-4

Numerical and Experimental Analysis of Influences of 1/*f* noises on Superconducting Integrated Circuits

*Yusuke Tsuna[1], Yuki Yamanashi[1,2], Nobuyuki Yoshikawa[1,2]

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Institute of Advanced Sciences, Yokohama National University[2]

Superconducting circuits such as a single flux quantum (SFQ) and a quantum flux parametron (QFP) circuits can operate with ultra-low power consumption. We have been numerically analyzing influences of the 1/*f* noise in the superconducting circuit using a conventional analog circuit simulator. To verify the numerical analysis results, we measure the gray-zone width of the QFP buffer, which corresponds to input dc current region that makes the logical decision be non-deterministic caused by the noises in the circuit. By comparing the numerically and experimentally obtained gray zone widths of the QFP buffer, the influence of the 1/*f* noise increases when the frequency of the excitation current is low. Moreover, we found that the influence of the 1/*f* noise on the QFP buffer is negligible above the 1 GHz operation.
Acknowledgment
This work was supported by JSPS KAKENHI Grant Number JP19H01945. The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2).

Keywords: 1/f noise, QFP circuit, grayzone

EDP2-5

Development of Majority-Logic-Based Top-Down Environment for Adiabatic Quantum-Flux-Parametron Circuits

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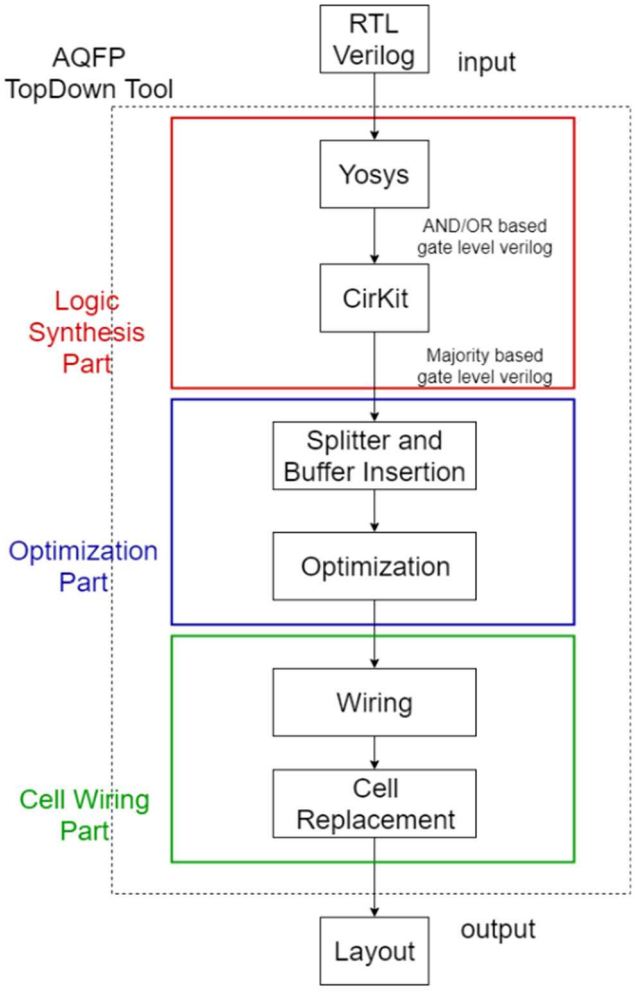
Electrical and Computer Engineering, Yokohama National University[1]
Institute of Advanced Sciences, Yokohama National University[2]

1 Abstract Adiabatic quantum-flux-parametron (AQFP) logic is one kind of superconducting logic family spotlighted as a technological foundation for developing extremely low-energy computers. However, AQFP circuits have a disadvantage in design time when compared with modern CMOS circuits because AQFP logic lacks adequate EDA tools. This is one of the major problems that must be solved to push AQFP logic into practical use. In this thesis, we show our top-down development flow, how to take advantage of a CMOS logic synthesis tool and convert it into an AQFP circuit. 2 Outline of AQFP Top-Down Design Tool There are roughly three parts of the AQFP top-down design tool: (1) logic synthesis; (2) logic optimization; (3) cell wiring. The logic synthesis part of the flow uses open source tools, whereas the other parts use tools that we have developed ourselves. The top-down design tool is a program that integrates all three of these parts. First, an RTL (register transfer level) Verilog file which describes the circuit's behavior is synthesized by a logic synthesis tool such as Yosys. The logic synthesize tool converts it to an AND/OR-based gate-level description. Next, it is converted to a majority-based netlist using CirKit. Second, the optimization part uses some tools we developed before. The synthesized circuit can not be used as it is, because the AQFP circuit is a phase-driven circuit. Gates such as“ splitter ”and“ buffer ”are needed to be inserted to line up and synchronize phases. We already developed a program to insert the necessary number of buffers and splitters while also considering retiming optimization to reduce the necessary number of phase-aligning buffers. This completed netlist is given to the physical optimization part which is implemented using the genetic algorithm. However, all signal/bias lines are just virtual connections at this stage. Finally, these connections are automatically replaced by each physical cells that are suitable for the place, size, and direction during the cell wiring part of the top-down flow. The AQFP top-down environment can be built by integrating these steps. It enables us to export a chip layout from an RTL Verilog description.



Keywords: AQFP, topdown, logic synthesis, retiming

EDP2-6

Design and evaluation of multi-bit-input single-flux-quantum autocorrelator system for astronomical data analysis

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Institute of Advanced Sciences, Yokohama National University[2]

In radio astronomy, a superconductor-insulator-superconductor (SIS) mixer are used to detect millimeter and sub-millimeter waves from the universe. For efficient observation, increasing in the viewing angle by integration of multiple SIS mixers into one refrigerator is important. However, because the amplifier that is placed in the low temperature stage and transmits signal to room-temperature electronics is required for each mixer, total power consumption increases. Therefore, the number of SIS mixers integrated into one refrigerator is limited. To solve this problem, integration of a single-flux-quantum (SFQ) analog-to-digital converter (ADC) and an autocorrelator into the low-temperature stage is promising. Because the SFQ ADC has high-sensitivity, the low-temperature amplifiers could be removed. Moreover, total power consumption of the system can be drastically reduced by employing the SFQ ADC and the SFQ autocorrelator that can operate at several GHz with ultra-low power consumption. In this study, as a prototype of the system, we designed and evaluated the performances of the SFQ ADC that converts the SIS output signal to 2-bit digital data, the SFQ autocorrelator that supports 2-bit signal inputs, and the SFQ binary counter that can be used as an integrator. All circuit components were designed and implemented using the AIST 10 kA/cm^2 Nb advanced process 2 (ADP2). The autocorrelator was designed using many exclusive-OR gates, the implementation cost of which is small compared to that of the CMOS circuit. The number of the Josephson junction of the autocorrelator, and the counter are 1322, and 169, respectively. The experimental results of the designed circuits will be presented.

Acknowledgment
This work was supported by JSPS KAKENHI Grant Number JP19H01945. The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the advanced process 2 (ADP2).

Keywords: SFQ circuits, radio astronomy, ADC, autocorrelator

EDP2-7

Adiabatic Quantum-Flux-Parametron Design-For-Testability Components for Large-Scale Digital Circuits

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PRESTO, Japan Science and Technology Agency, Japan[2]
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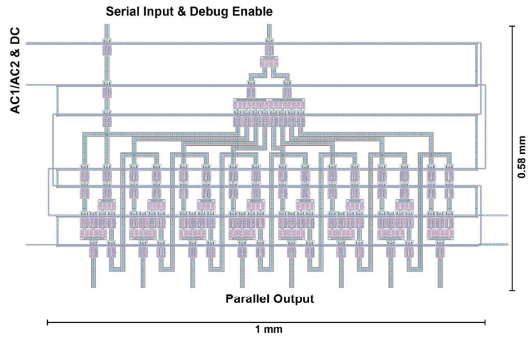
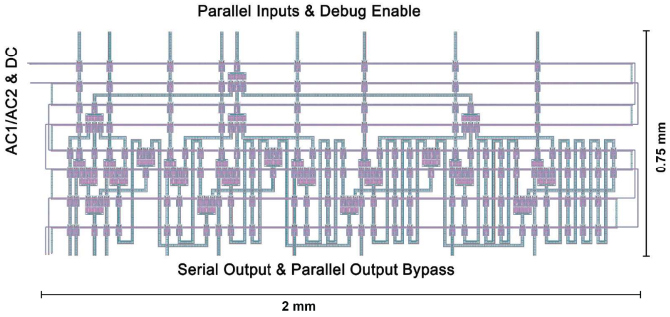
Adiabatic quantum-flux-parametron (AQFP) logic can operate with bit energies below $50k_BT$ at a clock frequency of 5 GHz, which makes it a suitable foundation for building energy-efficient computing systems. Complex circuits such as a microprocessor would benefit from additional circuitry to facilitate prototype testing during experimental measurement. Thus, we developed design-for-testability (DFT) components for use in the testing of an AQFP microprocessor, namely parallel-to-serial (P2S) and serial-to-parallel (S2P) data converters. These DFT components allow one to probe between processor sub-units while reducing the area overhead of I/O pads and off-chip interfaces typically needed to read-out intermediate signals. Because of the free-running, non-gated clock needed for AQFP, their design differs than that of their SFQ variants which have separate load and read control clocks. Instead, the AQFP variants use a debug control signal to isolate data of interest (in P2S) or block subsequent dataflow (in S2P) from interfering with the serialization/parallelization process. We developed 8-bit AQFP P2S/S2P units (~400 Josephson junctions and 1 mm^2 area each) and demonstrated fully correct operation.



Serial-to-Parallel Data Converter



Parallel-to-Serial Data Converter

Keywords: aqfp, design-for-testability, digital, microprocessor

EDP2-8

Investigation on the Method to Evaluate the Energy Dissipation of General Adiabatic Quantum-Flux-Parametron Logic Gates

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Adiabatic quantum-flux-parametron (AQFP) logic is an energy-efficient superconductor logic family. In previous numerical studies, we have evaluated the energy dissipation of basic AQFP logic gates, such as a buffer and a reversible logic gate, and demonstrated their sub-$k_B T$ switching energy, where k_B is the Boltzmann's constant and T is the temperature, by integrating the product of the excitation current and voltage associated with the gates over time. However, this method is not applicable to complex logic gates, especially those in which the number of inputs is different from that of outputs. In the present study, we establish a systematic method to evaluate the energy dissipation of general AQFP logic gates. In the proposed method, the energy dissipation is calculated by subtracting the energy dissipation of the peripheral circuits from that of the entire circuit. In this way, the energy change due to the interaction between gates, which makes it difficult to evaluate the energy dissipation, can be deducted. We evaluate the energy dissipation of a MAJ gate using this method.

Keywords: superconducting integrated circuit, adiabatic quanutum-flux-parametron, energy dissipation

EDP2-9

Energy Consumption of Half Flux Quantum Circuits Using π-Shifted Josephson Junctions

*Feng Li[1], Yuto Takeshita[1], Daiki Hasegawa[1], Kyosuke Sano[1], Masamitsu Tanaka[1], Taro Yamashita[1,2], Akira Fujimaki[1]

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We investigate energy consumption of the low-energy logic circuits called half flux quantum (HFQ) circuits, where half of a magnetic flux quantum ($\frac{1}{2}\Phi_0$) is used for the binary operation [1]. The HFQ circuits are made up of 0-π SQUIDs, which are composed of pairs of π-shifted Josephson junction (π-junction) and conventional Josephson junction (0-junction) with the same critical currents (I_c). In a 0-π SQUID, the π-junction, such as ferromagnetic Josephson junction, serves as both switching element and superconductor phase shift element. The HFQ circuits can also be implemented using SQUIDs composed of three π-junctions (π-π-π SQUIDs) or SQUIDs composed of two 0-junctions and one π-junction (0-0-π SQUIDs) instead of 0-π SQUIDs, where one π-junction is used for a non-switching, phase shift element and the other junctions are used for switching elements. Recently we successfully fabricated Nb/PdNi/Nb magnetic Josephson junctions on a four-layer Nb/AlO_x/Nb integrated circuit chips and obtained 0-0-π SQUIDs toward demonstration of HFQ circuits [2].
In the HFQ circuits, a SQUIDs act as Josephson junctions with an extremely small I_c if the SQUID loop inductance (L) is small, and lead to lower energy operation. In this study, we evaluate the energy consumption of HFQ circuits using numerical analysis and analog circuit simulation [3]. Fig. (a) shows a transmission line, basic wiring element of HFQ circuits composed of 0-π SQUIDs. The SQUID has two stable states where the loop current flows in clockwise or counterclockwise. The transmission line propagates a flip of the state in each SQUID. A π-leap in superconductor phase is observed at each single switching event, and dynamic energy (E_d) is consumed. We need the energy greater than the potential barrier between two states (ΔE) to switch a 0-π SQUID, and about twice the energy of ΔE is consumed under the optimal bias condition that maximizes the operating margin. The E_d corresponds to the product of $\frac{1}{2}\Phi_0$ and bias currents and is reduced below 0.1 aJ when $LI_c/\Phi_0 < 0.5$ using 100-μA junctions, as show in Fig. (b). We will report a comparison of energy consumption of HFQ circuits made up of the different type of SQUIDs.
[1] T. Kamiya et al. IEICE Trans. Electron. E101-C (2018) 385.
[2] D. Hasegawa et al. 17th Int. Supercond. Electron. Conf., 2019, Riverside, CA, USA.
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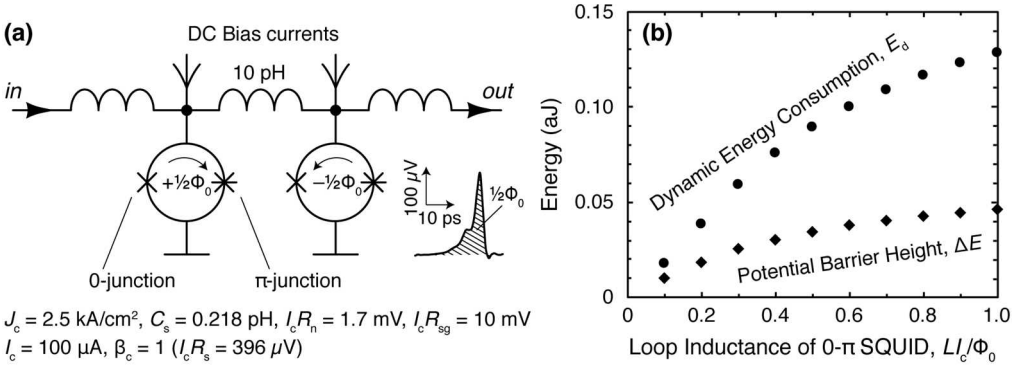

Fig. (a) Schematic diagram of HFQ transmission line, (b) loop inductance dependency of dynamic energy consumption and potential barrier height of a 0-π SQUID.

Keywords: Low-energy logic circuits, Ferromagnetic Josephson junction, π-shifted Josephson junction , Half flux quantum

EDP2-10

A Global Routing Method with Wire Length Budgeting for PTL Routing of SFQ Logic Circuits

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We propose a global routing method for the layout design of SFQ (Single-Flux-Quantum) logic circuits. In the proposed method, global routing is performed where coarse wiring routes are searched before detailed routing, and wire length is also budgeted to each net considering the available routing resources. This prevents the routing congestions caused by detouring routes for length matching during detailed routing of SFQ circuits and guarantees the routability.
In general, routing problem is solved in two steps called global routing and detailed routing because of the large complexity of the problem. Exact wiring routes are determined based on the global routing solution and therefore a global router should find a routing solution with high probability of routing completion.
The routing problem of SFQ circuits, however, cannot be solved by using the existing router because of its strict timing requirements. In SFQ circuits, wire length matching of PTLs (Passive Transmission Lines) is performed to meet the timing constraints, where shorter routes are detoured to extend the length. However, constraints and optimization objectives for SFQ circuits cannot be processed effectively by existing global routers, and the following detailed routing may fail.
To address this issue, we propose a global routing method with wire length budgeting. We focus on grid based global routing, where a given routing area is gridded into rectangular subregions and paths connecting them are searched to determine coarse wiring routes for given nets. In the proposed method, in addition to searching a path connecting subregions, wire length is also budgeted to each net at each subregion on the path. The successful length matching in detailed routing is guaranteed when a sufficiently long wire length is budgeted without excessive use of the given routing resources. We formulate our global routing problem and propose an algorithm to solve it. In our algorithm, routes are searched first, and an additional wire length is specified for each net considering the length matching constraints. Then, the wire length at each subregion on the path of each net is computed so that the specified additional wire length is budgeted while preventing the excessive use of routing resources.

Keywords: Single Flux Quantum, layout design, global routing, Passive Transmission Line

EDP2-11

Scan Design with Clockless Logic Gates for SFQ Circuits

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Digital logic testing of manufactured circuits is a time-consuming task. Design for testability (DFT) of circuits is essential for reducing test costs and improving test quality. One of the most popular DFT techniques for CMOS circuits is scan design that replaces flip-flops with scan flip-flops, inserts test points and increases testability. However, scan design is hardly adopted for Single-Flux-Quantum (SFQ) circuits while testability is an important issue because scan design with clocked logic gates can result in larger clock tree, deeper pipeline, more DFF insertions and larger chip area.
Clockless logic gates, which are logic gates without clock inputs, were proposed in [1]. In this paper, we adopt clockless logic gates rather than clocked logic gates for implementing combinational logic portion of circuits. Using clockless logic gates, SFQ circuits can be designed with small clock tree, shallow pipeline, a few DFF insertions and small chip area and thus scan design can be a practical option.
We propose scan flip-flops implemented with a D flip-flop with two readouts, confluence buffer and splitter. In our scan design, normal clock, scan data and scan clock signals are distributed to scan flip-flops and combinational blocks are composed of only clockless logic gates. A drawback of combinational block composed of clockless gates is that we cannot implement NOT function. To compensate this point, we propose inverting scan flip-flops.

[1] Kawaguchi, T., Tanaka, M., Takagi, K., & Takagi, N. (July, 2015). Demonstration of an 8-Bit SFQ Carry Look-Ahead Adder Using Clockless Logic Cells. In 2015 15th International Superconductive Electronics Conference (ISEC) (pp. 1-3). IEEE.

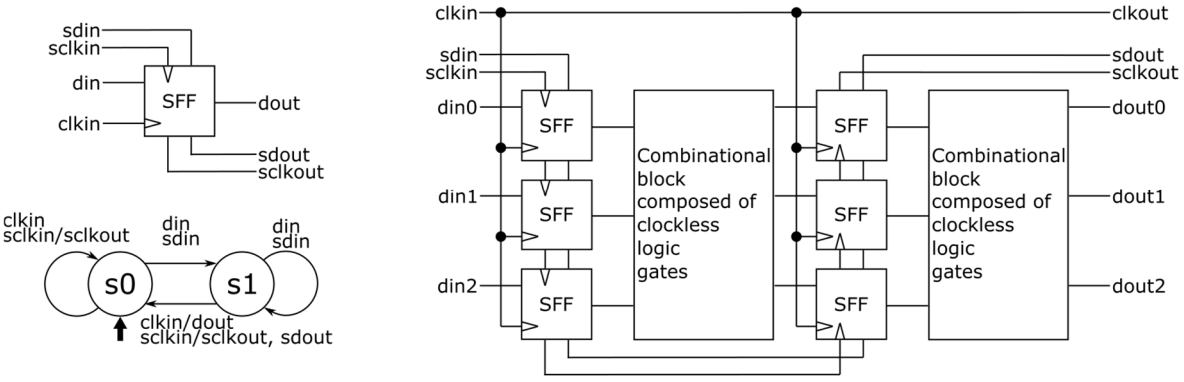

Fig. (a) Symbol and state transition diagram of proposed scan flip-flop (b) block diagram of proposed scan design

Keywords: SFQ circuit, scan flip-flop, clockless logic gates

EDP2-12

Investigation of the superconducting flux qubit for quantum annealing utilizing multi-layered Nb/AlOx/Nb Josephson junction technology

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A machine learning based on quantum computing is expected to be superior to the conventional machine learning in terms of high accuracy and learning time [1]. To build a superconducting quantum annealing computer suitable for the machine learning application, we have been investigated superconducting flux quantum bits (qubits) composed of the tunable rf-SQUID [2], which can be easily coupled to other qubits via magnetic coupling.
We evaluated a device consisting of the flux qubit and a dc-SQUID, Josephson junctions of which are resistively shunted, for read-out of the qubit state. The device was fabricated utilizing multi-layered Nb/AlOx/Nb Josephson junction technology, the AIST 2.5 kA/cm^2 Nb standard 2 process [3]. The critical currents of the Josephson junction were estimated to be 50 μA for the readout dc-SQUID and 50μA and 125μA for the qubit respectively. All measurements were carried out at 4.2 K. Figure 1 (a) shows a schematic of a circuit consisting of the flux qubit and the readout dc-SQUID. Since the qubit and the dc-SQUID are magnetically coupled by overlapping the qubit loop and the SQUID loop, the SQUID can read out the internal state of the qubit by applying appropriate bias current (I_{bias}) and flux (I_{flux}). To determine the appropriate bias condition for the readout dc-SQUID, the voltage response of the dc-SQUID was investigated. Figure 1 (b) shows dependences of the measured voltage on the I_{flux} when the I_{bias} of 0.7 mA and 1.2 mA were supplied. A periodic response, corresponding to applying the flux quantum Φ_o, was observed when I_{bias} of 1.2 mA was supplied. The voltage response of the readout dc-SQUID to magnetic flux applied to the qubit was measured by fixing the I_{bias} to be 0.04 mA (I_1). Figure 1(c) shows the measured voltage response as the function of magnetic flux applied to the qubit. We found the voltage response was digitalized. This indicates that the readout identifies the flux direction in the qubit.

Reference:
[1] S. Adachi and M. Henderson, arXiv :1510.06356, 2015.
[2] D. Saida et al., ISS 2018, ED4-5.
[3] M. Hidaka et al., Supercond. Sci. Technol., 19 S138–S142, 2006

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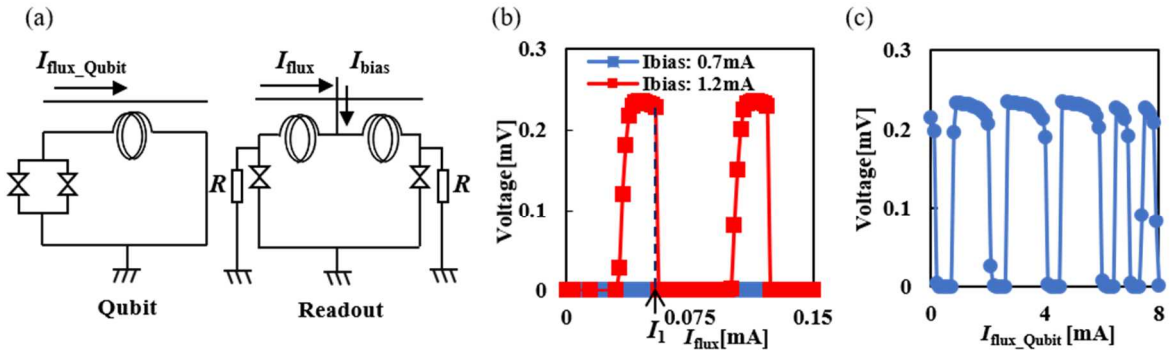

Fig.1 (a) Schematic circuit of readout having shunt resistances and qubit. (b) The readout voltage vs. applied I_{flux} at 4.2K measurement. (c) I_{flux_Qubit} dependence of the readout voltage.

Keywords: Superconducting flux qubit, Josephson junction (JJ), SQUID, Quantum annealing