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Logic Simulation Tool for RSFQ Circuits Accepting Arrivals of Multiple Pulses in a Clock Period

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RSFQ circuits and their energy-efficient derivatives are expected to realize high performance and energy-efficient computers. RSFQ circuits use pulse logic. Namely, voltage pulses are used for calculating logic functions.

Logic simulation of RSFQ logic circuits is carried out after designing layouts because the order of pulse arrivals at each gate affects its logic function and the order of pulse arrivals is determined in layout design. Though design exploration in logic design with logic simulation is necessary to obtain a reasonable design, it is difficult to evaluate various designs because designing a layout is a hard task. Methods to simulate a logic design before layout are crucial. A description method of RSFQ logic circuits was proposed. In the method, the order of pulse arrivals is annotated for each gate to represent the circuit behavior explicitly. A logic simulation tool for circuit descriptions based on the method has been also shown. The method and the tool are designed for simple designs. Designs with complex orders of pulse arrivals, i.e., appearances of multiple pulses at an input terminal during a clock period, cannot be represented with the method because it assumes at most one pulse arrives at an input terminal during a clock period.

Logic functions can be implemented with fewer logic gates by utilizing complex ordering of pulse arrivals. For example, a logic function “ab’+c” can be realized simply with a confluence buffer (CB) and a resettable D flip-flop (RDFF) having data, reset, and clock input terminals. Pulses of “a” and “c” are merged with a CB and are fed to the data terminal of an RDFF and a pulse of “b” is designed to be fed to its reset terminal between the pulse arrivals of “a” and “c.” This design cannot be described with the method.

The method to be proposed is an extension of the description method to treat designs with the complex ordering of pulse arrivals. The proposed method attaches a list for each input terminal of a gate to represent the order of pulse arrivals for multiple pulses for the terminal. The list for a pin contains integers to represent the order of pulses fed for the pin in a gate during a clock cycle.

A logic simulation tool was implemented. It is written in Python. With the tool, circuits with complex orders of pulse arrivals like the above example were simulated.

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