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Investigation of Thermal Resistance in a Cryopackage for Programmable Josephson Voltage Standard Device

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Since 2016, a programmable Josephson voltage standard (PJVS) system based on a liquid-helium-free cryocooler has been in practical use at NMIJ. In this system, however, there is a problem that the chip temperature slightly rises with the output voltage level, narrowing the bias-current margin for the PJVS device operation.

In our previous study, it was found that many voids existed in the solder layer used in our cryopackage and might be one of the possible causes for the temperature rise in the PJVS chip [1]. We investigated the void-ratio dependence of the thermal resistance both in the numerical simulations and the experimental measurements, and showed that the thermal resistance rapidly increases with the void ratio of greater than 80 %.

In this study, we are investigating more details of the void-ratio dependence and other measurements for the thermal resistance of our cryopackage for the PJVS device. Up to now, we found that the obtained data for the void-ratio dependence cannot be fitted by the simulated dependence, indicating the existence of a large residual thermal resistance of the order of 1 K/W or more (Fig. 1). We are now trying to reveal the cause for such the large thermal resistance.

[1] H. Takahashi, M. Maruyama, Y. Amagai, H. Yamamori, N. Kaneko, S. Kiryu, "Heat transfer analysis of a programmable Josephson voltage standard chip operated with a mechanical cooler," Physica C, Vol. 518, pp. 89-95, 1995.

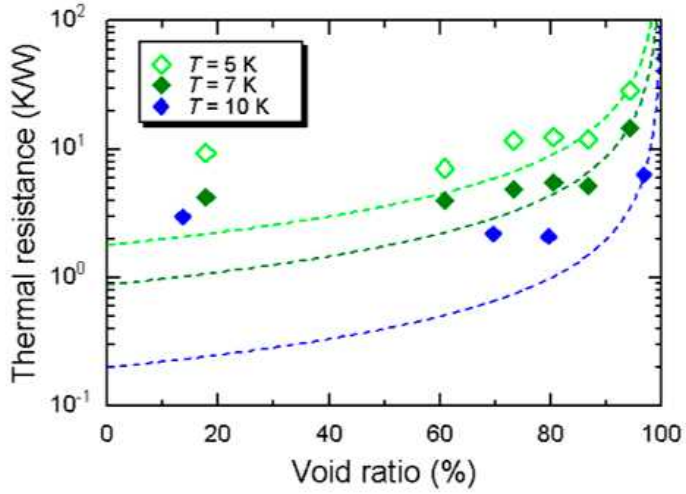

Fig. 1 Measured thermal resistances of the cryopackage for the PJVS device versus the void ratio in the solder layer. The broken lines indicate the fitting lines based on a simulation.

Keywords: Cryopackage, Josephson voltage standard, PJVS, Thermal resistance