EDP2-1

Design and Error-Rate Evaluation of RSFQ Logic Gates Comprising a Toggle Storage Loop

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RSFQ circuits are being investigated for microprocessor applications that take advantage of high-speed switching and low power consumption [1]. As the RSFQ circuit becomes larger, problems such as the complicated clock wiring, the increased bias current, and the increased magnetic field in the circuit adversely affect the circuit operation. Therefore, a simpler configuration is preferable for RSFQ logic cells. We have designed an area-reduced NOT-gate, in which a toggle storage loop is employed, for the purpose of reduction of these problems. Besides, bit error rate(BER) is another important indicator of the quality of digital transmission systems. In this paper, we evaluate the operation and BER of logic circuits including our area-reduced NOT gate.

The equivalent circuit of the area-reduced NOT gate is shown in fig. (a). Its NOT operation is as follows. When an SFQ is fed from the set terminal, J3 is switched to hold the SFQ in the J3-J4 storage loop. After another SFQ comes from the clock terminal, J4 is switched and the held SFQ is annihilated, which means no SFQ at the output terminal. When an SFQ is fed from the clock terminal without an SFQ in the J3-J4 storage loop, J6 is switched and the SFQ goes to the output terminal.

Test chips were fabricated using the Nb 2.5kA/cm^2 process(STP2) at the National Institute of Advanced Industrial Science and Technology(AIST), Japan.

The measurement was performed in a liquid helium bath. Fig. (b) shows the bias current versus BER for the 2.4×10^5 input of "0" and "1". No errors were observed for the bias current between 12.48mA and 13.71mA. Experimental results were fitted well with complementary error functions except for 2 points.

[1] e.g., Y. Ando, et. al., IEEE Trans. Appl. Supercond., **26**, (2016) 1301205.

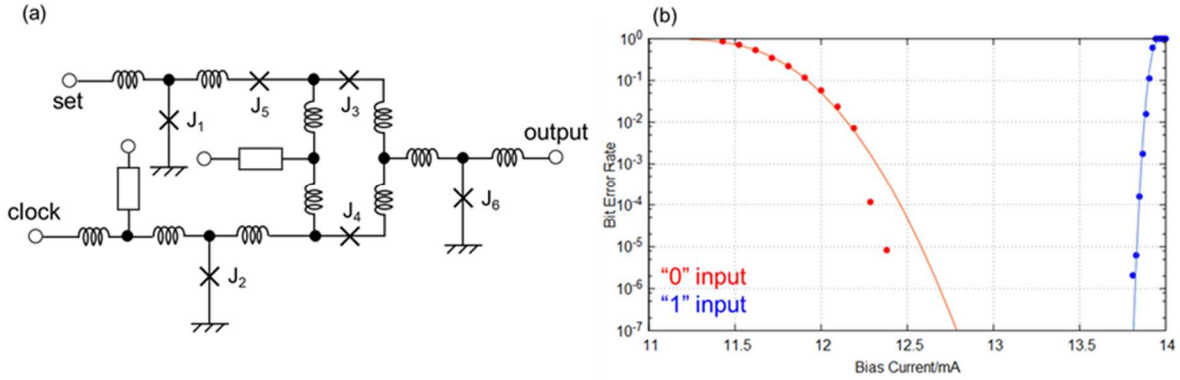

Fig. (a): Equivalent circuit of the are-reduced NOT-gate. (b): Experimental result and fitting curves of BER for the inputs of 2.4×10^5 "0" and "1"

Keywords: Nb integrated circuit, Bit-Error-Rate, RSFQ digital circuit