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Scan Design with Clockless Logic Gates for SFQ Circuits

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Digital logic testing of manufactured circuits is a time-consuming task. Design for testability (DFT) of circuits is essential for reducing test costs and improving test quality. One of the most popular DFT techniques for CMOS circuits is scan design that replaces flip-flops with scan flip-flops, inserts test points and increases testability. However, scan design is hardly adopted for Single-Flux-Quantum (SFQ) circuits while testability is an important issue because scan design with clocked logic gates can result in larger clock tree, deeper pipeline, more DFF insertions and larger chip area.
Clockless logic gates, which are logic gates without clock inputs, were proposed in [1]. In this paper, we adopt clockless logic gates rather than clocked logic gates for implementing combinational logic portion of circuits. Using clockless logic gates, SFQ circuits can be designed with small clock tree, shallow pipeline, a few DFF insertions and small chip area and thus scan design can be a practical option.
We propose scan flip-flops implemented with a D flip-flop with two readouts, confluence buffer and splitter. In our scan design, normal clock, scan data and scan clock signals are distributed to scan flip-flops and combinational blocks are composed of only clockless logic gates. A drawback of combinational block composed of clockless gates is that we cannot implement NOT function. To compensate this point, we propose inverting scan flip-flops.

[1] Kawaguchi, T., Tanaka, M., Takagi, K., & Takagi, N. (July, 2015). Demonstration of an 8-Bit SFQ Carry Look-Ahead Adder Using Clockless Logic Cells. In 2015 15th International Superconductive Electronics Conference (ISEC) (pp. 1-3). IEEE.

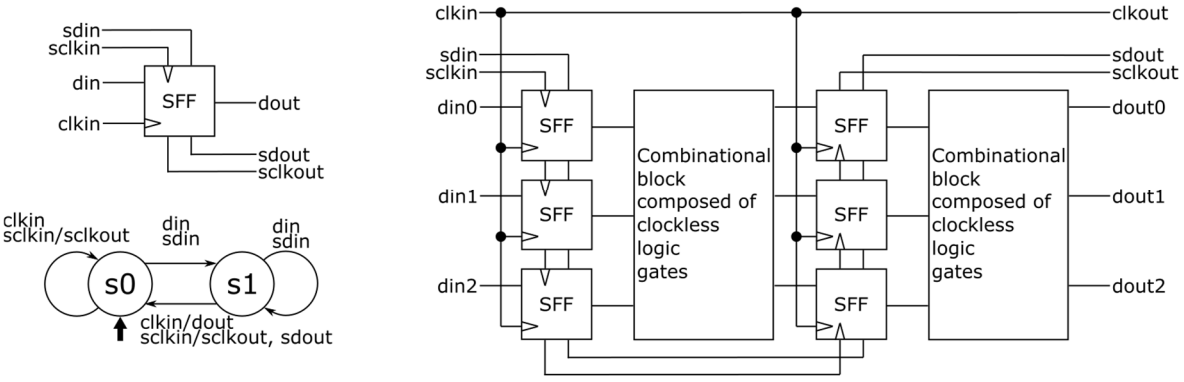

Fig. (a) Symbol and state transition diagram of proposed scan flip-flop (b) block diagram of proposed scan design

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