ED4-1-INV

EDA for Superconducting Circuits

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Superconducting integrated circuits have long been completely handcrafted or at best designed with a loose collection of tools that require manual manipulation of data and design transfer between tools. Electronic Design Automation (EDA) software development requires significant investment of resources to track the evolution of integrated circuit fabrication processes, which has only been possible commercially for highly successful semiconductor integrated circuit processes. The IARPA SuperTools project which started in 2017 is the largest known investment to date made in superconducting EDA tool development. SuperTools is divided into two main categories: high-level tools for the synthesis of digital logic circuits, clock networks and placed-and-routed layouts for systems such as processors with millions of logic gates; and physical-level tools for the design, simulation, optimization, verification, layout and parameter extraction of devices and digital logic cells with the inclusion of fabrication process simulation. In this paper the physical-level tools are presented by way of a design example, from device characterization through logic circuit conception and design to layout verification and cell library sign-off.

ED4-2-INV

Superconducting SFQ Circuits Research Progress in China

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Although it has been about 30 years since the birth of superconducting circuits, research activities on them have remained quietly in China, if not none, until recently. The first wafer-level single flux quantum (SFQ) process in China appeared about 3 years ago at SIMIT. Since then, we have gone through several upgrades and changes. Corresponding design and measurement infrastructure have been developed on site simultaneously to enable close-loop feedback research cycles. In particular, we have established process control monitor (PCM) analysis for the latest SIMIT Nb03 SFQ process, and carried out systematically measurement and verification of cell libraries optimized for this process and move towards benchmark circuits demonstration, such as shift register, frequency divider and so on. Besides, EDA tools for optimization and buildup of SFQ cell libraries: model, behavior and timing libraries, as well as automatic placement and routing for large scale SFQ circuits design have been developed. In this report, we will present these latest progresses.

Keywords: SFQ, SFQ process, EDA Tools

ED4-3-INV

Performance Improvement of Superconducting Circuit by Introducing π-Shifted Josephson Junctions

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Hybridization of Josephson junctions (JJs) and π-shifted Josephson junction (π-JJs), which induces the static superconducting phase shift of π across the junction, is one of effective methods to improve the performance of superconducting integrated circuits. We can reduce circuit area of the superconducting circuits by replacing the large inductances with the π-JJs. Moreover, we can drastically simplify the circuit structure of superconducting flip-flop with complementally outputs by using a symmetric storage loop composed of both the JJ and the π-JJ. We will discuss the improvement of performances of superconducting circuits by introducing π-JJs into the conventional superconducting circuits quantitatively in terms of the circuit area, the operating margin, and the operating frequency on the basis of the analog circuit simulations by the PJSIM we developed. We will show a possible application to superconducting single-flux-quantum containing π-JJs to dual-rail circuit that can remove static power consumption.

Keywords: SFQ circuit, π-Josephson junction, circuit simulator

ED4-4

Enhanced Voltage Swing of RSFQ Output Amplifiers Equipped with Double-Stack SQUIDs

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We have enhanced voltage swing of an RSFQ distributed amplifier by replacing a SQUID, which works as a voltage generator, with a double-stack SQUID. A double-stack SQUID is a 4-junction SQUID with two superconducting loop. In other words, it is composed of two stacked SQUIDs sharing a sensing inductor. Because of its stack structure, a double-stack SQUID is expected to generate two-fold output voltage. We have designed 4-, 12-, and 24-stage RSFQ distributed amplifiers equipped with 4, 12, and 24 double-stack SQUIDs, respectively. The fundamental cell, of which the dimensions are 80 by 80 μm², is compatible with an RSFQ digital cell library referred to as "CONNECT." Test chips were fabricated using a 25-μA/μm² Nb integration process of the National Institute of Advanced Industrial Science and Technology, which was referred to as the AIST STP2. In measurements, a test chip was cooled in a liquid helium bath. The experimental output voltage swings of 4-, 12- and 24-stage RSFQ distributed amplifiers were up to 2.93, 8.34, and 14.50 mV, respectively.

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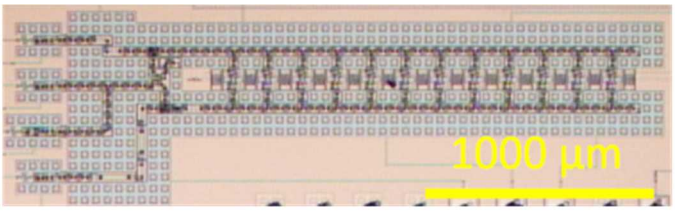

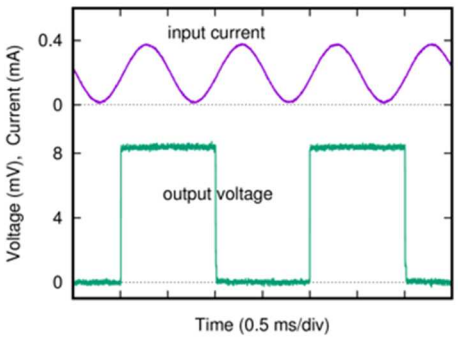

Fig. Photomicrograph and operation waveforms of a 12-stage RSFQ output amplifier equipped with double-stack SQUIDs.

Keywords: distributed amplifier, Nb/AlOx/Nb, RSFQ digital circuits, IO interface

ED4-5

Logic Simulation Tool for RSFQ Circuits Accepting Arrivals of Multiple Pulses in a Clock Period

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RSFQ circuits and their energy-efficient derivatives are expected to realize high performance and energy-efficient computers. RSFQ circuits use pulse logic. Namely, voltage pulses are used for calculating logic functions.

Logic simulation of RSFQ logic circuits is carried out after designing layouts because the order of pulse arrivals at each gate affects its logic function and the order of pulse arrivals is determined in layout design. Though design exploration in logic design with logic simulation is necessary to obtain a reasonable design, it is difficult to evaluate various designs because designing a layout is a hard task. Methods to simulate a logic design before layout are crucial. A description method of RSFQ logic circuits was proposed. In the method, the order of pulse arrivals is annotated for each gate to represent the circuit behavior explicitly. A logic simulation tool for circuit descriptions based on the method has been also shown. The method and the tool are designed for simple designs. Designs with complex orders of pulse arrivals, i.e., appearances of multiple pulses at an input terminal during a clock period, cannot be represented with the method because it assumes at most one pulse arrives at an input terminal during a clock period.

Logic functions can be implemented with fewer logic gates by utilizing complex ordering of pulse arrivals. For example, a logic function “ab’+c” can be realized simply with a confluence buffer (CB) and a resettable D flip-flop (RDFF) having data, reset, and clock input terminals. Pulses of “a” and “c” are merged with a CB and are fed to the data terminal of an RDFF and a pulse of “b” is designed to be fed to its reset terminal between the pulse arrivals of “a” and “c.” This design cannot be described with the method.

The method to be proposed is an extension of the description method to treat designs with the complex ordering of pulse arrivals. The proposed method attaches a list for each input terminal of a gate to represent the order of pulse arrivals for multiple pulses for the terminal. The list for a pin contains integers to represent the order of pulses fed for the pin in a gate during a clock cycle.

A logic simulation tool was implemented. It is written in Python. With the tool, circuits with complex orders of pulse arrivals like the above example were simulated.

Keywords: Rapid Single Flux Quantum Circuits, Logic Simulation, Design Automation

ED4-6

Design and High-speed Test of an SFQ-based Single-chip FFT Processor

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Fast Fourier transform (FFT) processor is custom hardware for computing discrete Fourier transform (DFT) at high speed, where DFT can convert a signal from a time domain to a frequency domain, and is widely used in digital signal processing. High-performance FFT processors based on single flux quantum (SFQ) circuits are attractive in many fields because of their high-speed operation with low power consumption [1]. In our previous study, we have designed and implemented a 4-bit 8-point SFQ FFT processor using the AIST 10 kA/cm^2 Nb advanced processor (ADP 2.2) [2] and confirmed the correct operation of the first stage at low-speed test [3]. In this study, we designed a 7-bit 8-point SFQ-based single-chip FFT processor and fabricated it using the ADP 2.2 process. The correct operation of the FFT processor was confirmed at the on-chip high-speed test [4]. We input 8-point discrete time-domain signals such as a sine wave and a cosine wave and demonstrated the spectrum analysis ability of the FFT processor. The FFT processor can perform 2.55×10^{11} times of FFT calculations per Joule at the maximum frequency of 47.8GHz, where it takes 7.4 ns for one time of FFT calculation. We also evaluated the energy efficiency of a 32-bit 64-point SFQ FFT processor and compared it with that of a CMOS FFT processor under a 45 nm technology. We confirmed it is two orders of magnitude better than that of the CMOS FFT processor with serial architecture.

Keywords: single flux quantum circuits, FFT, processor, superconducting