EDP2-1

Design and Error-Rate Evaluation of RSFQ Logic Gates Comprising a Toggle Storage Loop

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RSFQ circuits are being investigated for microprocessor applications that take advantage of high-speed switching and low power consumption [1]. As the RSFQ circuit becomes larger, problems such as the complicated clock wiring, the increased bias current, and the increased magnetic field in the circuit adversely affect the circuit operation. Therefore, a simpler configuration is preferable for RSFQ logic cells. We have designed an area-reduced NOT-gate, in which a toggle storage loop is employed, for the purpose of reduction of these problems. Besides, bit error rate(BER) is another important indicator of the quality of digital transmission systems. In this paper, we evaluate the operation and BER of logic circuits including our area-reduced NOT gate.

The equivalent circuit of the area-reduced NOT gate is shown in fig. (a). Its NOT operation is as follows. When an SFQ is fed from the set terminal, J3 is switched to hold the SFQ in the J3-J4 storage loop. After another SFQ comes from the clock terminal, J4 is switched and the held SFQ is annihilated, which means no SFQ at the output terminal. When an SFQ is fed from the clock terminal without an SFQ in the J3-J4 storage loop, J6 is switched and the SFQ goes to the output terminal.

Test chips were fabricated using the Nb 2.5kA/cm^2 process(STP2) at the National Institute of Advanced Industrial Science and Technology(AIST), Japan.

The measurement was performed in a liquid helium bath. Fig. (b) shows the bias current versus BER for the 2.4×10^5 input of "0" and "1". No errors were observed for the bias current between 12.48mA and 13.71mA. Experimental results were fitted well with complementary error functions except for 2 points.

[1] e.g., Y. Ando, et. al., IEEE Trans. Appl. Supercond., **26**, (2016) 1301205.

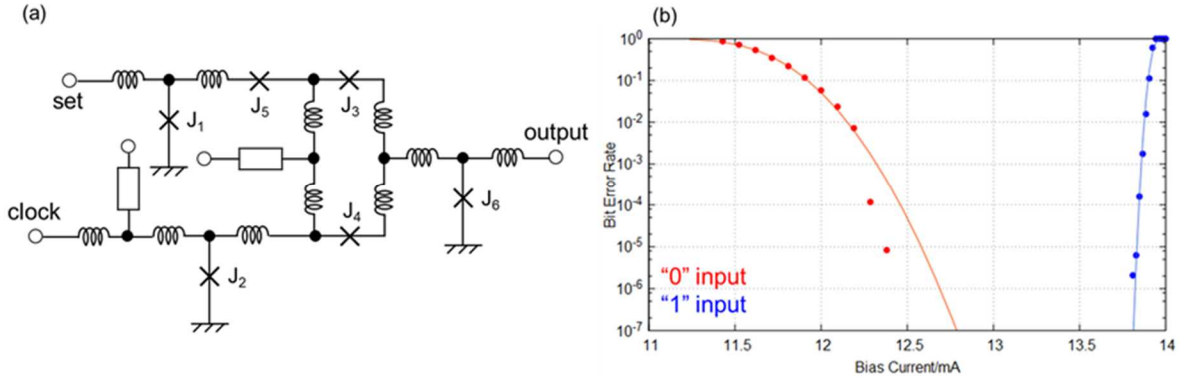

Fig. (a): Equivalent circuit of the are-reduced NOT-gate. (b): Experimental result and fitting curves of BER for the inputs of 2.4×10^5 "0" and "1"

Keywords: Nb integrated circuit, Bit-Error-Rate, RSFQ digital circuit

EDP2-2

Single-Flux-Quantum Parallel Multiplier Using Accumulator Unit

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A multiplier is one of fundamental circuit elements for digital circuits. So far, single-flux-quantum (SFQ) multipliers based on various hardware algorithms have been investigated. Conventional SFQ multipliers required relatively large circuit areas because the adder tree is used to sum partial products. In this study, we investigated and designed a new SFQ parallel multiplier that uses a parallel accumulator unit. Because the accumulator unit, which is composed of resettable toggle flip-flops, can be used as the parallel counter, the circuit area for summation of partial products can be drastically reduced. We designed and simulated a 4-bit SFQ parallel multiplier based on the investigated hardware algorithm using the AIST 10 kA/cm^2 Nb advanced process. The target operating frequency is 30 GHz. The multiplier can be used as a multiplier-accumulator (MAC). Thought the operating frequency of the designed multiplier is slightly lower than that of the conventional SFQ parallel multiplier, the circuit area can be reduced. The number of Josephson junction to implement 4-bit multiplier is 1374, which is approximately half of that of the conventional 4-bit SFQ parallel multiplier.

Acknowledgment
This work was supported by JSPS KAKENHI Grant Number JP 18K04280. The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the advanced process 2 (ADP2).

Keywords: SFQ circuits, multiplier, accumulator, adder;MAC

EDP2-3

Investigation of influence by flux trapping for interconnection of adiabatic quantum-flux-parametron circuits

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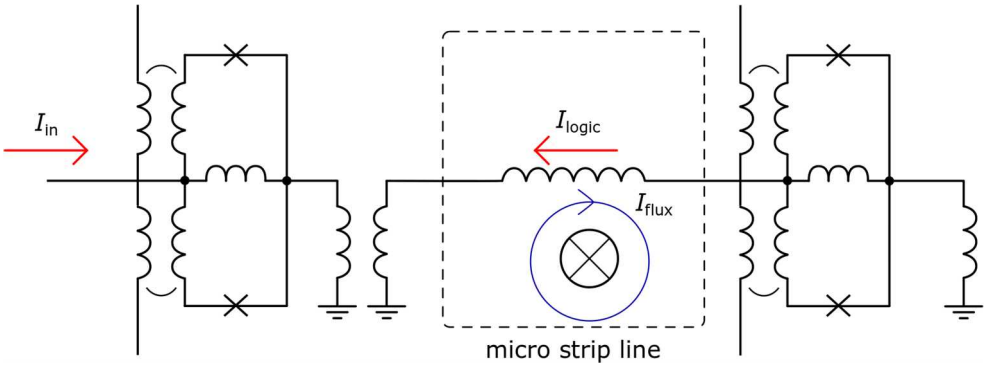
Adiabatic quantum-flux-parametron (AQFP) logic is known as an energy efficient superconductor digital logic family [1]. When compared to the state-of the-art CMOS technology, AQFP has a high advantage in term of power consumption. To realize large scale AQFP integrated circuit, many studies are ongoing [2][3].
One problem that has recently emerged is low yield of circuits with complex interconnect. One possible cause is magnetic flux trapping. A trapped magnetic flux is a physical phenomenon that occurs mainly in the ground layer. When a normal conduction region is surrounded by a superconducting one, permanent current flows around that region. The current and magnetic flux are thought to affect the circuit and cause malfunctions.
The logic state of an AQFP circuit is encoded as the direction of current, and each AQFP gate are connected by a superconducting stripline. The amplitude of the data signal current maybe smaller than the circular current that is generated by the trapped flux, especially for long, complex interconnect whose large parasitic inductance already attenuates the AQFP current output. Therefore, circuit malfunctions may happen as the data current signal is negatively influenced by trapped flux along the interconnect, resulting in the incorrect sampling of data in the receiving AQFP gate.
It is very difficult to completely avoid magnetic flux trapping. One solution is adapting moats along the interconnection. Moats are done by creating slits in the ground plane, and by creating defects such that trapped flux are guided to the moat [4]. In this time, we designed a test circuit with the application of various moat structures and considered its effectiveness in AQFP circuits.

[1] Takeuchi, N., Ehara, K., Inoue, K., Yamanashi, Y., & Yoshikawa, N., IEEE Transactions on Applied Superconductivity, 23(3), 1700304–1700304 (2013).
[2] Yamae, T., Takeuchi, N. & Yoshikawa, N., Supercond. Sci. Technol. 32, 035005 (2019).
[3] Cai, R. et al., in Proceedings of the 46th International Symposium on Computer Architecture 567–578 (ACM, 2019).
[4] Polyakov, Y., Narayana, S. & Semenov, V. K., IEEE Trans. Appl. Supercond. 17, 520–525 (2007).



Keywords: Superconducting integrated circuit, Adiabatic Quantum Flux Prametron, Flux Trapping

EDP2-4

Numerical and Experimental Analysis of Influences of 1/*f* noises on Superconducting Integrated Circuits

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Superconducting circuits such as a single flux quantum (SFQ) and a quantum flux parametron (QFP) circuits can operate with ultra-low power consumption. We have been numerically analyzing influences of the 1/*f* noise in the superconducting circuit using a conventional analog circuit simulator. To verify the numerical analysis results, we measure the gray-zone width of the QFP buffer, which corresponds to input dc current region that makes the logical decision be non-deterministic caused by the noises in the circuit. By comparing the numerically and experimentally obtained gray zone widths of the QFP buffer, the influence of the 1/*f* noise increases when the frequency of the excitation current is low. Moreover, we found that the influence of the 1/*f* noise on the QFP buffer is negligible above the 1 GHz operation.
Acknowledgment
This work was supported by JSPS KAKENHI Grant Number JP19H01945. The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2).

Keywords: 1/f noise, QFP circuit, grayzone

EDP2-5

Development of Majority-Logic-Based Top-Down Environment for Adiabatic Quantum-Flux-Parametron Circuits

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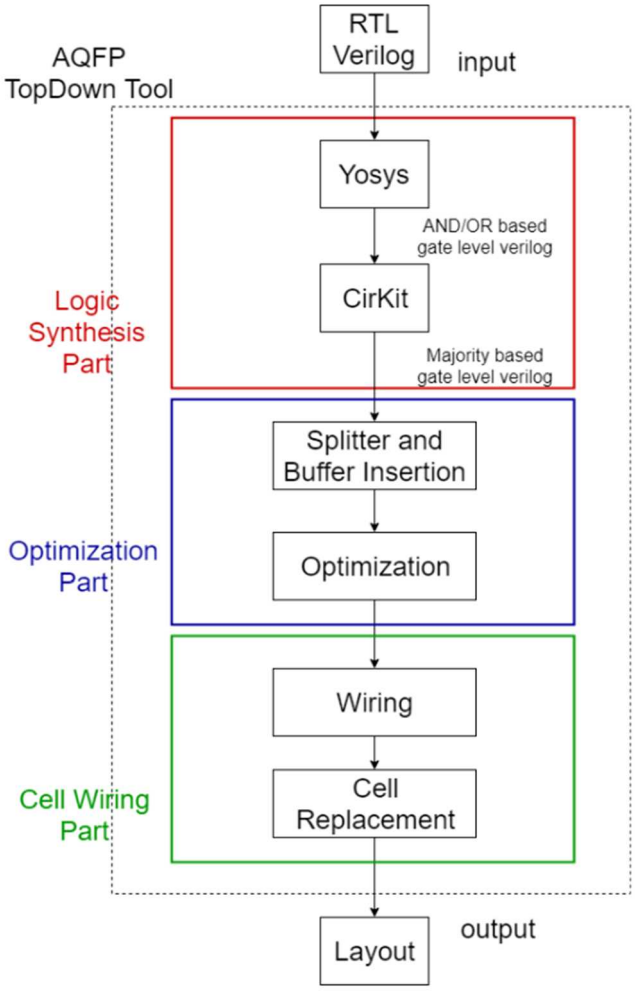
1 Abstract Adiabatic quantum-flux-parametron (AQFP) logic is one kind of superconducting logic family spotlighted as a technological foundation for developing extremely low-energy computers. However, AQFP circuits have a disadvantage in design time when compared with modern CMOS circuits because AQFP logic lacks adequate EDA tools. This is one of the major problems that must be solved to push AQFP logic into practical use. In this thesis, we show our top-down development flow, how to take advantage of a CMOS logic synthesis tool and convert it into an AQFP circuit. 2 Outline of AQFP Top-Down Design Tool There are roughly three parts of the AQFP top-down design tool: (1) logic synthesis; (2) logic optimization; (3) cell wiring. The logic synthesis part of the flow uses open source tools, whereas the other parts use tools that we have developed ourselves. The top-down design tool is a program that integrates all three of these parts. First, an RTL (register transfer level) Verilog file which describes the circuit's behavior is synthesized by a logic synthesis tool such as Yosys. The logic synthesize tool converts it to an AND/OR-based gate-level description. Next, it is converted to a majority-based netlist using CirKit. Second, the optimization part uses some tools we developed before. The synthesized circuit can not be used as it is, because the AQFP circuit is a phase-driven circuit. Gates such as“ splitter ”and“ buffer ”are needed to be inserted to line up and synchronize phases. We already developed a program to insert the necessary number of buffers and splitters while also considering retiming optimization to reduce the necessary number of phase-aligning buffers. This completed netlist is given to the physical optimization part which is implemented using the genetic algorithm. However, all signal/bias lines are just virtual connections at this stage. Finally, these connections are automatically replaced by each physical cells that are suitable for the place, size, and direction during the cell wiring part of the top-down flow. The AQFP top-down environment can be built by integrating these steps. It enables us to export a chip layout from an RTL Verilog description.



Keywords: AQFP, topdown, logic synthesis, retiming

EDP2-6

Design and evaluation of multi-bit-input single-flux-quantum autocorrelator system for astronomical data analysis

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In radio astronomy, a superconductor-insulator-superconductor (SIS) mixer are used to detect millimeter and sub-millimeter waves from the universe. For efficient observation, increasing in the viewing angle by integration of multiple SIS mixers into one refrigerator is important. However, because the amplifier that is placed in the low temperature stage and transmits signal to room-temperature electronics is required for each mixer, total power consumption increases. Therefore, the number of SIS mixers integrated into one refrigerator is limited. To solve this problem, integration of a single-flux-quantum (SFQ) analog-to-digital converter (ADC) and an autocorrelator into the low-temperature stage is promising. Because the SFQ ADC has high-sensitivity, the low-temperature amplifiers could be removed. Moreover, total power consumption of the system can be drastically reduced by employing the SFQ ADC and the SFQ autocorrelator that can operate at several GHz with ultra-low power consumption. In this study, as a prototype of the system, we designed and evaluated the performances of the SFQ ADC that converts the SIS output signal to 2-bit digital data, the SFQ autocorrelator that supports 2-bit signal inputs, and the SFQ binary counter that can be used as an integrator. All circuit components were designed and implemented using the AIST 10 kA/cm^2 Nb advanced process 2 (ADP2). The autocorrelator was designed using many exclusive-OR gates, the implementation cost of which is small compared to that of the CMOS circuit. The number of the Josephson junction of the autocorrelator, and the counter are 1322, and 169, respectively. The experimental results of the designed circuits will be presented.

Acknowledgment
This work was supported by JSPS KAKENHI Grant Number JP19H01945. The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the advanced process 2 (ADP2).

Keywords: SFQ circuits, radio astronomy, ADC, autocorrelator

EDP2-7

Adiabatic Quantum-Flux-Parametron Design-For-Testability Components for Large-Scale Digital Circuits

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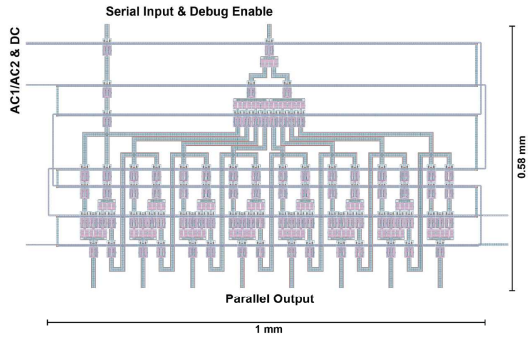
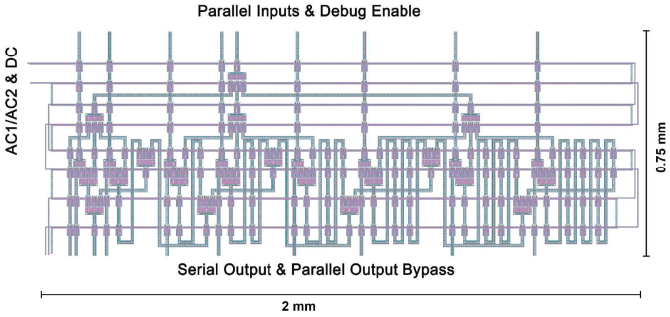
Adiabatic quantum-flux-parametron (AQFP) logic can operate with bit energies below $50k_BT$ at a clock frequency of 5 GHz, which makes it a suitable foundation for building energy-efficient computing systems. Complex circuits such as a microprocessor would benefit from additional circuitry to facilitate prototype testing during experimental measurement. Thus, we developed design-for-testability (DFT) components for use in the testing of an AQFP microprocessor, namely parallel-to-serial (P2S) and serial-to-parallel (S2P) data converters. These DFT components allow one to probe between processor sub-units while reducing the area overhead of I/O pads and off-chip interfaces typically needed to read-out intermediate signals. Because of the free-running, non-gated clock needed for AQFP, their design differs than that of their SFQ variants which have separate load and read control clocks. Instead, the AQFP variants use a debug control signal to isolate data of interest (in P2S) or block subsequent dataflow (in S2P) from interfering with the serialization/parallelization process. We developed 8-bit AQFP P2S/S2P units (~400 Josephson junctions and 1 mm^2 area each) and demonstrated fully correct operation.



Serial-to-Parallel Data Converter



Parallel-to-Serial Data Converter

Keywords: aqfp, design-for-testability, digital, microprocessor

EDP2-8

Investigation on the Method to Evaluate the Energy Dissipation of General Adiabatic Quantum-Flux-Parametron Logic Gates

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Adiabatic quantum-flux-parametron (AQFP) logic is an energy-efficient superconductor logic family. In previous numerical studies, we have evaluated the energy dissipation of basic AQFP logic gates, such as a buffer and a reversible logic gate, and demonstrated their sub-$k_B T$ switching energy, where k_B is the Boltzmann's constant and T is the temperature, by integrating the product of the excitation current and voltage associated with the gates over time. However, this method is not applicable to complex logic gates, especially those in which the number of inputs is different from that of outputs. In the present study, we establish a systematic method to evaluate the energy dissipation of general AQFP logic gates. In the proposed method, the energy dissipation is calculated by subtracting the energy dissipation of the peripheral circuits from that of the entire circuit. In this way, the energy change due to the interaction between gates, which makes it difficult to evaluate the energy dissipation, can be deducted. We evaluate the energy dissipation of a MAJ gate using this method.

Keywords: superconducting integrated circuit, adiabatic quanutum-flux-parametron, energy dissipation

EDP2-9

Energy Consumption of Half Flux Quantum Circuits Using π-Shifted Josephson Junctions

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JST-PRESTO[2]

We investigate energy consumption of the low-energy logic circuits called half flux quantum (HFQ) circuits, where half of a magnetic flux quantum ($\frac{1}{2}\Phi_0$) is used for the binary operation [1]. The HFQ circuits are made up of 0-π SQUIDs, which are composed of pairs of π-shifted Josephson junction (π-junction) and conventional Josephson junction (0-junction) with the same critical currents (I_c). In a 0-π SQUID, the π-junction, such as ferromagnetic Josephson junction, serves as both switching element and superconductor phase shift element. The HFQ circuits can also be implemented using SQUIDs composed of three π-junctions (π-π-π SQUIDs) or SQUIDs composed of two 0-junctions and one π-junction (0-0-π SQUIDs) instead of 0-π SQUIDs, where one π-junction is used for a non-switching, phase shift element and the other junctions are used for switching elements. Recently we successfully fabricated Nb/PdNi/Nb magnetic Josephson junctions on a four-layer Nb/AlO_x/Nb integrated circuit chips and obtained 0-0-π SQUIDs toward demonstration of HFQ circuits [2].
In the HFQ circuits, a SQUIDs act as Josephson junctions with an extremely small I_c if the SQUID loop inductance (L) is small, and lead to lower energy operation. In this study, we evaluate the energy consumption of HFQ circuits using numerical analysis and analog circuit simulation [3]. Fig. (a) shows a transmission line, basic wiring element of HFQ circuits composed of 0-π SQUIDs. The SQUID has two stable states where the loop current flows in clockwise or counterclockwise. The transmission line propagates a flip of the state in each SQUID. A π-leap in superconductor phase is observed at each single switching event, and dynamic energy (E_d) is consumed. We need the energy greater than the potential barrier between two states (ΔE) to switch a 0-π SQUID, and about twice the energy of ΔE is consumed under the optimal bias condition that maximizes the operating margin. The E_d corresponds to the product of $\frac{1}{2}\Phi_0$ and bias currents and is reduced below 0.1 aJ when $LI_c/\Phi_0 < 0.5$ using 100-μA junctions, as show in Fig. (b). We will report a comparison of energy consumption of HFQ circuits made up of the different type of SQUIDs.
[1] T. Kamiya et al. IEICE Trans. Electron. E101-C (2018) 385.
[2] D. Hasegawa et al. 17th Int. Supercond. Electron. Conf., 2019, Riverside, CA, USA.
[3] Y. Yamanashi et al, Supercond. Sci. Technol. 31 (2018) 105003.
Acknowledgments: This work was supported by the JSPS KAKENHI, Grant Numbers JP18H05211, JP18H01498, and JP19H05615, and JST MIRAI JPMJMI18E1.

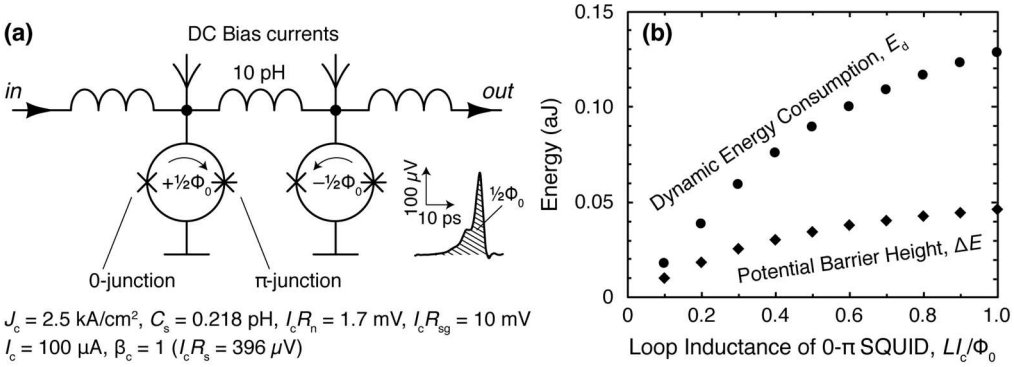

Fig. (a) Schematic diagram of HFQ transmission line, (b) loop inductance dependency of dynamic energy consumption and potential barrier height of a 0-π SQUID.

Keywords: Low-energy logic circuits, Ferromagnetic Josephson junction, π-shifted Josephson junction , Half flux quantum

EDP2-10

A Global Routing Method with Wire Length Budgeting for PTL Routing of SFQ Logic Circuits

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Graduate School of Engineering, Mie University, Japan[2]

We propose a global routing method for the layout design of SFQ (Single-Flux-Quantum) logic circuits. In the proposed method, global routing is performed where coarse wiring routes are searched before detailed routing, and wire length is also budgeted to each net considering the available routing resources. This prevents the routing congestions caused by detouring routes for length matching during detailed routing of SFQ circuits and guarantees the routability.
In general, routing problem is solved in two steps called global routing and detailed routing because of the large complexity of the problem. Exact wiring routes are determined based on the global routing solution and therefore a global router should find a routing solution with high probability of routing completion.
The routing problem of SFQ circuits, however, cannot be solved by using the existing router because of its strict timing requirements. In SFQ circuits, wire length matching of PTLs (Passive Transmission Lines) is performed to meet the timing constraints, where shorter routes are detoured to extend the length. However, constraints and optimization objectives for SFQ circuits cannot be processed effectively by existing global routers, and the following detailed routing may fail.
To address this issue, we propose a global routing method with wire length budgeting. We focus on grid based global routing, where a given routing area is gridded into rectangular subregions and paths connecting them are searched to determine coarse wiring routes for given nets. In the proposed method, in addition to searching a path connecting subregions, wire length is also budgeted to each net at each subregion on the path. The successful length matching in detailed routing is guaranteed when a sufficiently long wire length is budgeted without excessive use of the given routing resources. We formulate our global routing problem and propose an algorithm to solve it. In our algorithm, routes are searched first, and an additional wire length is specified for each net considering the length matching constraints. Then, the wire length at each subregion on the path of each net is computed so that the specified additional wire length is budgeted while preventing the excessive use of routing resources.

Keywords: Single Flux Quantum, layout design, global routing, Passive Transmission Line

EDP2-11

Scan Design with Clockless Logic Gates for SFQ Circuits

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Digital logic testing of manufactured circuits is a time-consuming task. Design for testability (DFT) of circuits is essential for reducing test costs and improving test quality. One of the most popular DFT techniques for CMOS circuits is scan design that replaces flip-flops with scan flip-flops, inserts test points and increases testability. However, scan design is hardly adopted for Single-Flux-Quantum (SFQ) circuits while testability is an important issue because scan design with clocked logic gates can result in larger clock tree, deeper pipeline, more DFF insertions and larger chip area.
Clockless logic gates, which are logic gates without clock inputs, were proposed in [1]. In this paper, we adopt clockless logic gates rather than clocked logic gates for implementing combinational logic portion of circuits. Using clockless logic gates, SFQ circuits can be designed with small clock tree, shallow pipeline, a few DFF insertions and small chip area and thus scan design can be a practical option.
We propose scan flip-flops implemented with a D flip-flop with two readouts, confluence buffer and splitter. In our scan design, normal clock, scan data and scan clock signals are distributed to scan flip-flops and combinational blocks are composed of only clockless logic gates. A drawback of combinational block composed of clockless gates is that we cannot implement NOT function. To compensate this point, we propose inverting scan flip-flops.

[1] Kawaguchi, T., Tanaka, M., Takagi, K., & Takagi, N. (July, 2015). Demonstration of an 8-Bit SFQ Carry Look-Ahead Adder Using Clockless Logic Cells. In 2015 15th International Superconductive Electronics Conference (ISEC) (pp. 1-3). IEEE.

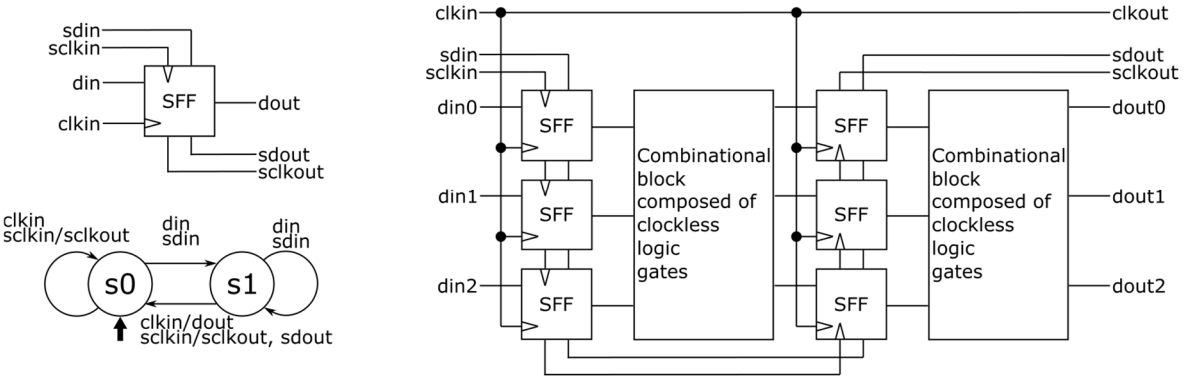

Fig. (a) Symbol and state transition diagram of proposed scan flip-flop (b) block diagram of proposed scan design

Keywords: SFQ circuit, scan flip-flop, clockless logic gates

EDP2-12

Investigation of the superconducting flux qubit for quantum annealing utilizing multi-layered Nb/AlOx/Nb Josephson junction technology

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A machine learning based on quantum computing is expected to be superior to the conventional machine learning in terms of high accuracy and learning time [1]. To build a superconducting quantum annealing computer suitable for the machine learning application, we have been investigated superconducting flux quantum bits (qubits) composed of the tunable rf-SQUID [2], which can be easily coupled to other qubits via magnetic coupling.
We evaluated a device consisting of the flux qubit and a dc-SQUID, Josephson junctions of which are resistively shunted, for read-out of the qubit state. The device was fabricated utilizing multi-layered Nb/AlOx/Nb Josephson junction technology, the AIST 2.5 kA/cm^2 Nb standard 2 process [3]. The critical currents of the Josephson junction were estimated to be 50 μA for the readout dc-SQUID and 50μA and 125μA for the qubit respectively. All measurements were carried out at 4.2 K. Figure 1 (a) shows a schematic of a circuit consisting of the flux qubit and the readout dc-SQUID. Since the qubit and the dc-SQUID are magnetically coupled by overlapping the qubit loop and the SQUID loop, the SQUID can read out the internal state of the qubit by applying appropriate bias current (I_{bias}) and flux (I_{flux}). To determine the appropriate bias condition for the readout dc-SQUID, the voltage response of the dc-SQUID was investigated. Figure 1 (b) shows dependences of the measured voltage on the I_{flux} when the I_{bias} of 0.7 mA and 1.2 mA were supplied. A periodic response, corresponding to applying the flux quantum Φ_o, was observed when I_{bias} of 1.2 mA was supplied. The voltage response of the readout dc-SQUID to magnetic flux applied to the qubit was measured by fixing the I_{bias} to be 0.04 mA (I_1). Figure 1(c) shows the measured voltage response as the function of magnetic flux applied to the qubit. We found the voltage response was digitalized. This indicates that the readout identifies the flux direction in the qubit.

Reference:
[1] S. Adachi and M. Henderson, arXiv :1510.06356, 2015.
[2] D. Saida et al., ISS 2018, ED4-5.
[3] M. Hidaka et al., Supercond. Sci. Technol., 19 S138–S142, 2006

Acknowledgement: The devices were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2).

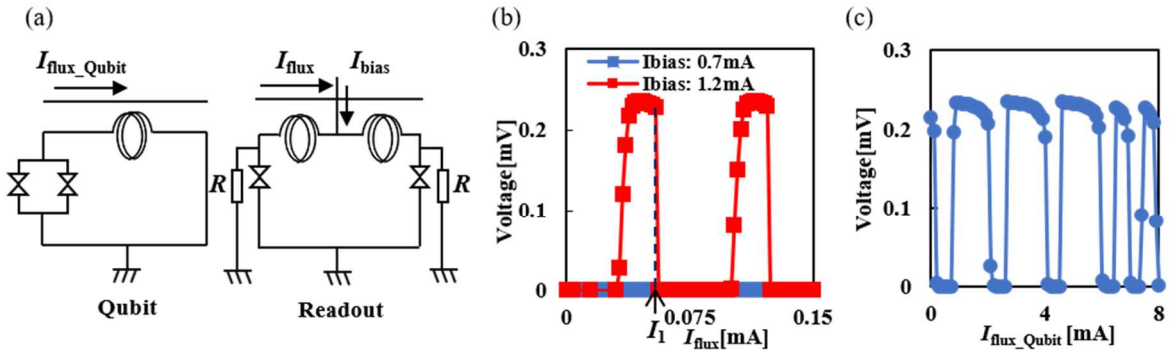

Fig.1 (a) Schematic circuit of readout having shunt resistances and qubit. (b) The readout voltage vs. applied I_{flux} at 4.2K measurement. (c) I_{flux_Qubit} dependence of the readout voltage.

Keywords: Superconducting flux qubit, Josephson junction (JJ), SQUID, Quantum annealing